Analog Module Architecture for Space-Qualified Field-Programmable Mixed-Signal Arrays

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September 27, 1999

Abstract

Spacecraft require all manner of both digital and analog circuits. Onboard digital systems are constructed almost exclusively from field-programmable gate array (FPGA) circuits providing numerous advantages over discrete design including high integration density, high reliability, fast turn-around design cycle time, lower mass, volume, and power consumption, and lower parts acquisition and flight qualification costs. Analog and mixed-signal circuits perform tasks ranging from housekeeping to signal conditioning and processing. These circuits are painstakingly designed and built using discrete components due to a lack of options for field-programmability. FPAA (Field-Programmable Analog Array) and FPMA (Field-Programmable Mixed-signal Array) parts exist [1] but not in radiation-tolerant technology and not necessarily in an architecture optimal for the design of analog circuits for spaceflight applications.

This paper outlines an architecture proposed for an FPAA fabricated in an existing commercial digital CMOS process used to make radiation-tolerant antifuse-based FPGA devices. The primary concerns are the impact of the technology and the overall array architecture on the flexibility of programming, the bandwidth available for high-speed analog circuits, and the accuracy of the components for high-performance applications.

1 Introduction

The ability to use radiation-tolerant programmable digital logic parts in hardware intended for use in high-reliability space missions provides significant cost savings. The savings result partly from shorter design cycles and lower risk, but mostly from reduced parts acquisition and flight qualification costs. Without these parts, many projects would be unable to afford custom gate array implementations, and would be forced to resort to discrete component designs with the accompanying increase of system size, mass, and power consumption.

A simliar situation exists in the mixed-signal field today. Almost all spacecraft contain numerous moderate-performance analog and digital processing and I/O circuits. These circuits, used for applications such as status monitoring, motor and temperature control, and signal conditioning and processing, are widely distributed throughout the spacecraft. Traditionally, these mixed-signal circuits have been implemented almost exclusively using discrete components, because the cost savings are not significant enough to justify a custom ASIC design. However, the resources used by such circuits, including mass, power, and volume, add up very quickly. The ability to implement such designs using general-purpose, programmable analog or mixed-signal arrays would be advantageous in all respects, analogous to the advantages gained using a Field-Programmable Gate Array (FPGA) for digital circuits: lower parts acquisition and qualification costs, higher levels of integration, lower power consumption, fast turn-around time for design cycles, and improved reliability.

The Field-Programmable Analog Array (FPAA) is the analog equivalent of the FPGA, a digital programmable device such as those made by companies such as Actel, Xilinx, and Altera. Unlike FPGAs, which contain a large number of modules and interconnections allowing arbitrary configurations of combinatorial and sequential logic, FPAA devices typically contain a small number of CABs (Configurable Analog Blocks). The resources of each CAB varies widely between different commercially available and research devices. FPAAs directed toward standard analog design typically feature a CAB containing an operational amplifer, programmable capacitor arrays (PCAs), and either programmable resistor arrays for continuous-time circuits or configurable switches for switched-capacitor circuits [1].

A Field-Programmable Mixed-signal Array (FPMA) is comprised of digital, analog, and interface modules. In many ways, an FPMA is a more useful device than the FPAA is by itself, due to the extensive use of digital for communications throughout the spacecraft and between the spacecraft and Earth. Almost all analog circuits on board the spacecraft require interfacing to digital systems, and again there are numerous advantages to locating the interface circuitry within a field-programmable part. The digital portion of an FPMA can be relatively small and allows simple digital processing to take place close to the analog signal source without requiring a separate FPGA for the purpose.

2 Analog Circuits in Digital Technology

Our proposed analog module architecture is intended for implementation in a CMOS fabrication technology featuring antifuse (one-time programmable) interconnections. Processes with antifuse capability are digital processes used by the FPGA industry, some of which meet the stringent requirements of radiation tolerance for spaceflight applications. However, they are not well suited to traditional analog circuit design, and so necessitate careful consideration of the analog module design and architecture. Fortunately, this aspect of analog design has been a primary focus of research in recent years due to the wide availability of digital processes and the shrinking availability of dedicated analog processes. This research has produced, for instance, a wide variety of designs for CMOS operational amplifiers maintaining a wide dynamic range while constrained by a low power supply voltage, and designs having good power supply rejection (PSRR), an important consideration in an FPMA architecture where noise from the digital modules will invariably couple into the analog modules.

A major constraint of analog VLSI design in a digital process is the requirement for linear capacitors. Field-programmability adds the constraint that fabricated capacitors must have a large capacitance per unit area, so that a sufficient number of programmable capacitor arrays (PCAs) will fit on a single chip of area comparable to standard FPGAs. Capacitors add in parallel, so a PCA with 6 bits of precision is made of 63 equal parts (see Figure 1), each of which must have a capacitance significantly larger than the parasitic capacitances associated with the substrate and the interconnect. This accounts for the fact that PCAs occupy the largest amount of area on an FPAA or FPMA.

Some analog fabrication processes feature two layers of polysilicon for the purpose of creating linear capacitors. Digital processes usually lack this feature, and often the "traditional" metal-polysilicon structure has such low capacitance per unit area that it requires far more die area than can be practically allocated to capacitor arrays. The capacitance associated with the polysilicon-diffusion interface of MOS transistors is typically the largest interlayer capacitance available in a process, but is nonlinear as a function of both voltage and frequency, as shown in Figure 2 [2]. When operated in the accumulation mode, the capacitance is both linear and maximum. However, around the transistor's threshold voltage, the capacitance drops due to capacitive division across the transistor channel.

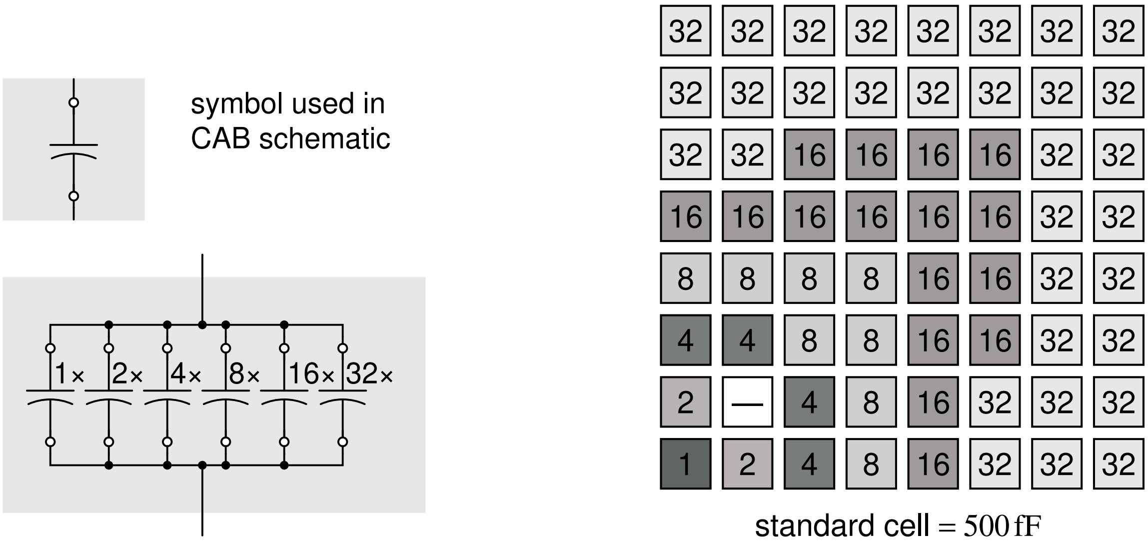

Figure 1: 6-bit Programmable Capacitor Array (PCA).

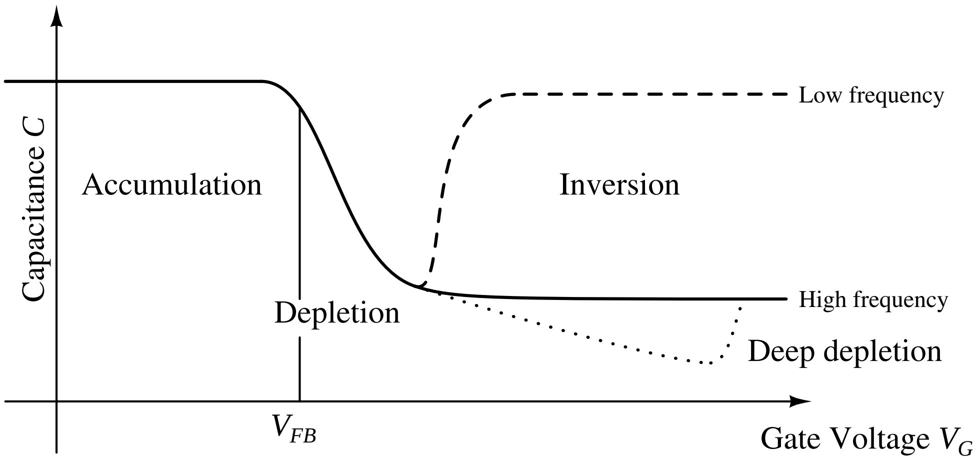

Figure 2: Nonlinear characteristic of a MOS capacitor.

Fortunately, there are several methods available to alleviate the nonlinearity problem [3]. The structure of Figure 3 is one which uses diffusion of the same carrier type as the well surrounding to create the capacitor bottom. This MOS structure, which cannot be used as a transistor, displays the same nonlinear capacitive behavior as the graph of Figure 2, but shifted to the right, which increases the voltage range in which the device operates in the accumulation mode.

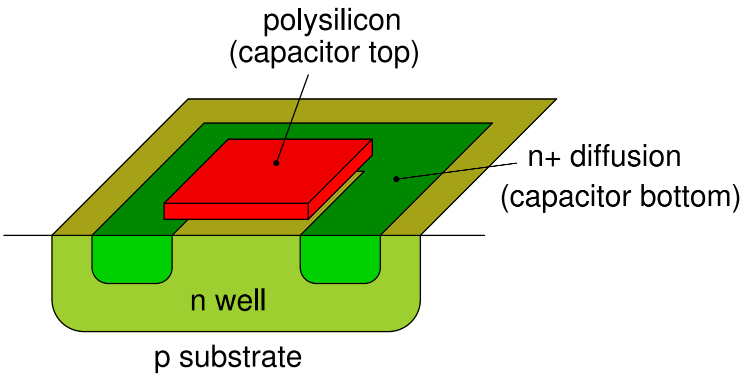

Figure 3: Structure of an accumulation-mode MOS capacitor.

The design solution of Figure 4 [3] is one which can be used when an analog switched-capacitor design requires a voltage across a MOS capacitor large enough to take the device out of accumulation mode and into the region of nonlinear capacitance. Because switched-capacitor designs require resetting the voltage across capacitors to reference values during a portion of the clock cycle, two capacitors can be placed back-to-back with the voltage between them set, during the refresh period, to a bias value ensuring accumulation-mode operation. During the remainder of the cycle, the shared node is decoupled from the bias, and the two capacitors behave like a single linear capacitor.

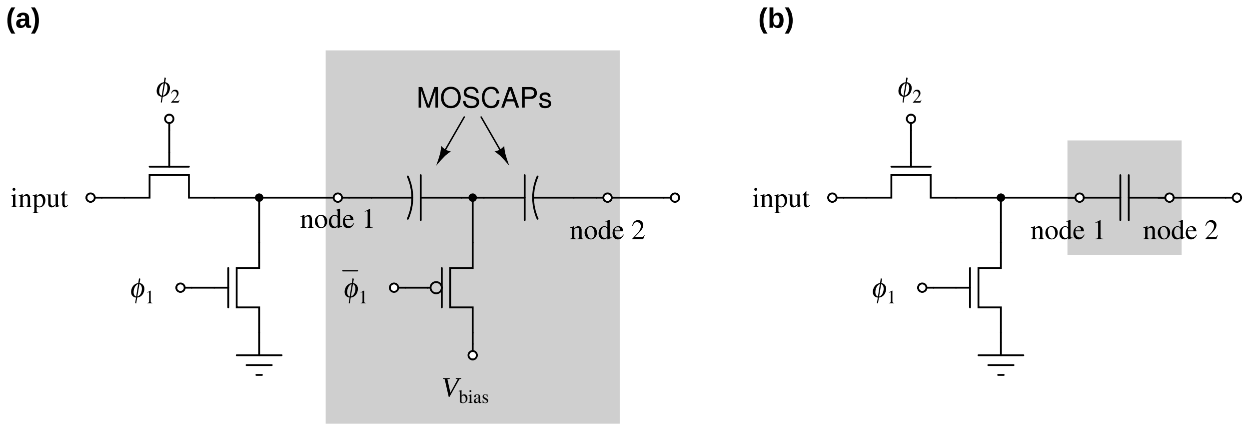

Figure 4: Design of a linearized MOS capacitor structure for switched-capacitor circuits. When clocked and biased correctly, circuits **(a)** and **(b)** are equivalent.

3 Interconnections

Interconnection resistance is proportional to signal delay, and is probably the most likely reason for the rarity of FPAA parts commercially available. All known FPAA architectures to date [1] have used RAM-based interconnect, in which two interconnection networks are connected by a MOS transistor acting as a switch. Switch resistance across such a device is typically in the range of 1000 to 5000 Ω.

Switched-capacitor circuits require MOS transistor switches, and several experimental architectures have taken advantage of that fact, getting double duty from the charge-transfer switches by using them as interconnect switches as well [4]. Consequently, there is no loss of bandwidth over and above what is normally associated with switched-capacitor circuits.

Nevertheless, modern metal-to-metal (M2M) antifuse technology [5] achieves resistances as low as 15 to 25 Ω per antifuse, which is an order of magnitude below the previous generation of antifuses and two orders of magnitude below MOS switches. Actel Corporation incorporates M2M antifuses into several chip series, most notably the RT-SX line of radiation-tolerant chips suitable for many spaceflight applications [6]. Use of M2M antifuse interconnects potentially allows fast (at least 10 to 20 MHz) continuous-time circuits to be built with field-programmable modules. By contrast, a switched-capacitor circuit requires a clock frequency 50 to 100 times the maximum required bandwidth of the equivalent continuous-time circuit. To make use of continuous-time circuits, the analog array architecture must incorporate programmable resistor arrays in addition to the programmable capacitor arrays. Unfortunately, resistance tolerances are not well-controlled in digital processes, so the extent to which the FPAA architecture can be applied to continuous-time circuit design is questionable.

4 Array Architecture

In an attempt to answer questions about the viability of an FPAA using antifuse technology in a digital process, we have designed a test structure to be fabricated on the Actel RT-SX process, incorporating twelve analog modules in a 3×4 array, which will allow us to test both continuous-time and switched-capacitor designs of numerous standard spaceflight applications, including pulse shaping, analog-to-digital and digital-to-analog conversion, modulators, oscillators, and filters.

The design of a single block incorporates circuit components as resources which can be connected into the circuit individually using antifuses. When unprogrammed, the resources are decoupled from the circuit except through the small antifuse capacitance. Our FPAA analog module design contains the following resources:

- 1 operational amplifier
- 4 programmable resistors
- 8 progammable capacitor arrays (6-bit resolution)
- 32 complementary MOS switches

The operational amplifier is a two-stage differential design for a digital process published in Yoshizawa, et al. [3], modified as necessary to meet design rules and maintain stability over the range of output loading capacitances possible with programming of the PCA. A continuous-time, rather than switched-capacitor, circuit performs common-mode feedback (CMFB); it consumes more power but allows the amplifier to be used in continuous-time as well as switched-capacitor circuit configurations. In a production version it would be desirable to reprogram the amplifier circuit for optimum performance under varying conditions, such as speed for use as a comparator.

Figure 1 shows the programmable capacitor array schematic used. Figure 5 shows the remainder of the resources, while Figure 6 shows one side of the differential analog block architecture (apart from the amplifier, one side is a mirror image of the other). Antifuse connections are not shown in the figure. Note that the row of switch resources acts as a barrier between the analog signal routing network and the digital signal

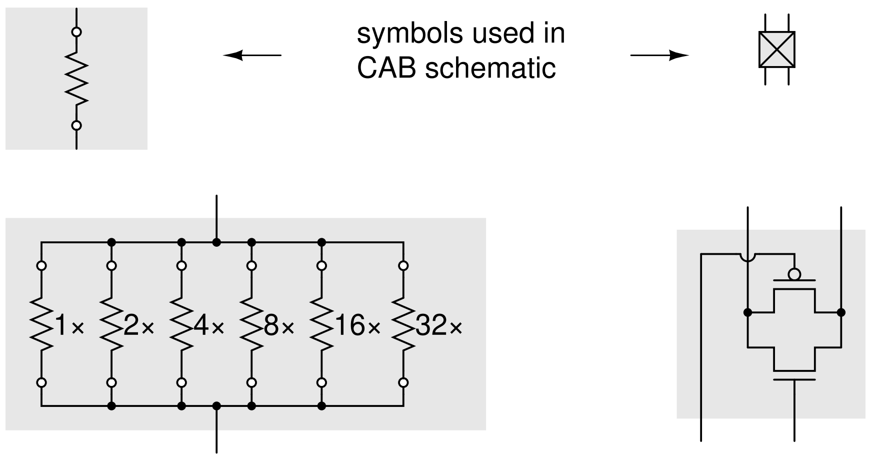

Figure 5: Programmable resistor and switch resources.

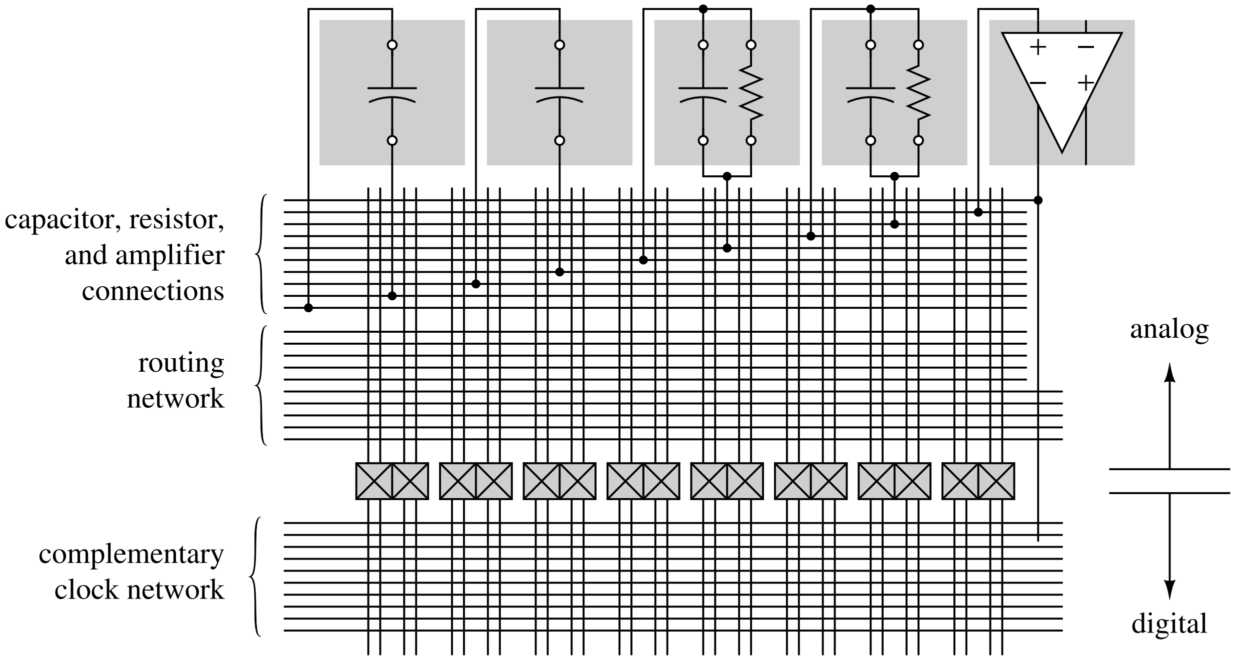

Figure 6: Configurable Analog Block (CAB) (only one side of differential architecture shown).

routing network, helping to reduce digital noise coupling to the analog portion of the FPAA. Figure 7 shows two complete CABs as connected in one column of the test chip, including the vertical routing network and the antifuse connections.

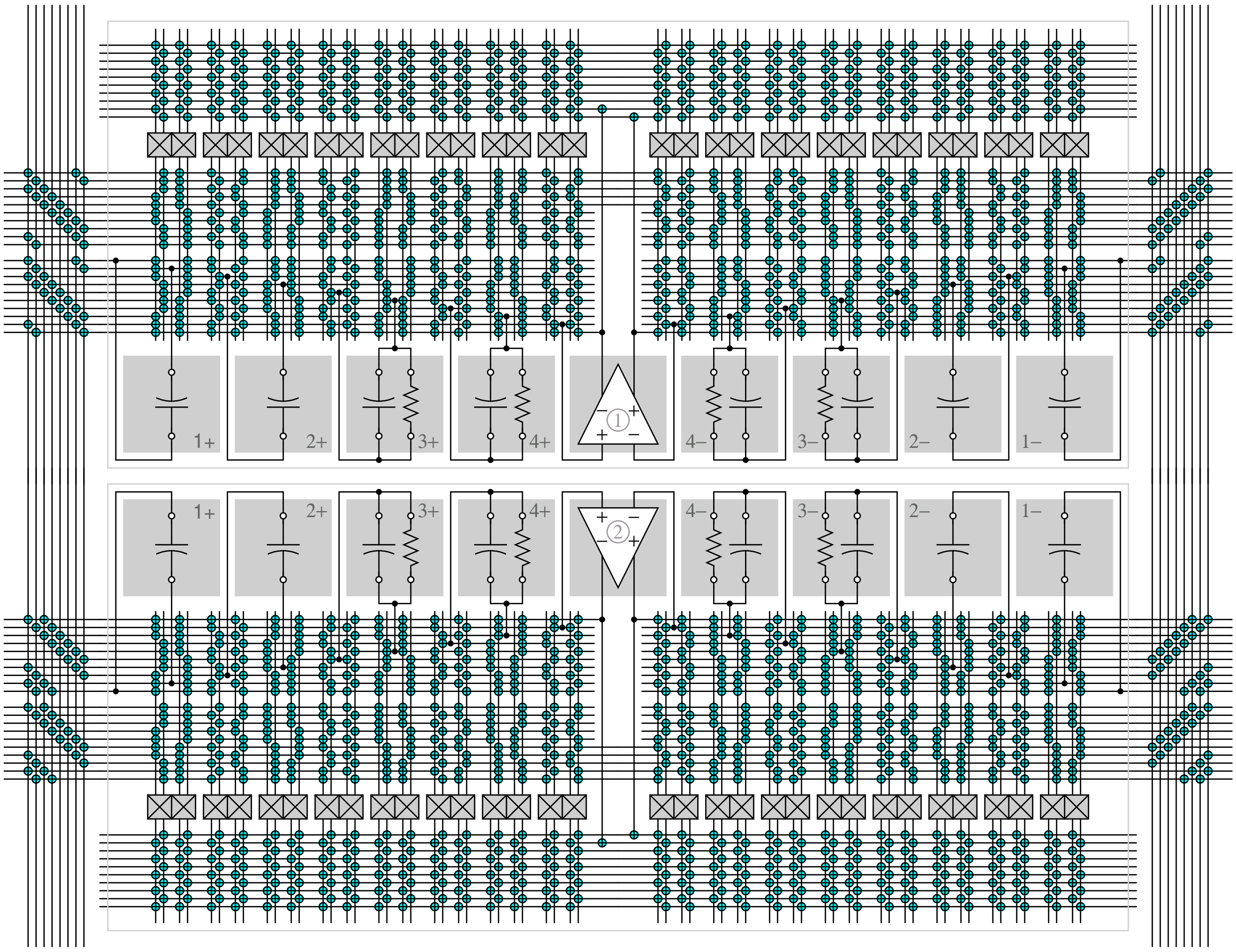

Figure 7: Architecture of the FPAA test chip, showing one column containing two CABs, with routing network and antifuses.

5 Conclusions

The recent spotlight on FPAA research and development shows a continued interest and need for such devices in spite of a continued lack of commercially-available options. Still, what is possibly the greatest potential target for FPAA/FPMA technology—radiation-tolerant and high-reliability areas such as space flight hardware—has not been addressed. Field-Programmable Analog and Mixed-Signal Arrays could replace discrete component circuits in tasks ranging from housekeeping to signal conditioning and processing, resulting in lower costs, weight, and power consumption, and significantly shorter time for design cycles and flight qualification.

Research on novel architectures for field-programmable analog arrays [1, 4] provides us with fast and efficient array designs. Other research [3] provides circuits and layout considerations for linear capacitors in a digital process when used in a switched-capacitor framework. In the commercial sector, new advances in antifuse technology [5] with low-resistance interconnections allow speed and bandwidth previously not possible in field-programmable circuits. All indications are that the coupling of high-speed interconnect technology with efficient FPAA designs and analog techniques for digital processes will produce viable programmable chips to meet the needs of spacecraft designers.

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