The Analog Wavelet Chip for Speech Compression

Chip Specifications

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Abstract

This paper describes the implementation in CMOS technology of a circuit which performs analog wavelet decompositions of a one-dimensional (e.g., sound) input. The circuit is based on the Analog VLSI techniques described by Carver Mead in *Analog VLSI and Neural Systems* [1]. The analog wavelet outputs are the output of a logarithmically scaled set of bandpass filters; each band is to be sampled (externally) at a rate proportional to the Nyquist rate of the highest frequency content of that band. The result is a matrix of discrete points describing the input signal as a function of both frequency and time. The filter function of each band is gaussian shaped in order to best resolve the uncertainty relation between time and frequency at each sampled point. This chip has been designed by Tim Edwards under the direction of Michael Godfrey, and fabricated by MOSIS. Zilog Corporation of Campbell, California, provided the funding for this project.

1 Overview

This paper describes the Analog Wavelet Transform chip, a CMOS subthreshold circuit design intended for use in an experimental speech compression system. This chip was built as an alternative to using a computer or DSP system to perform the same calculations; the advantages of this approach are reduced size and power consumption. The resulting analog implementation is inflexible in terms of ability to reprogram the function performed, and requires dealing with the problem of temperature sensitivity, variable process parameters, and noise injection throughout the circuit. However, we believe that the circuit will be effective for speech signals and will be smaller and cheaper than the digital alternatives.

The theory behind the Continuous Wavelet Transform has been treated in earlier papers. This paper seeks to describe in full the most recent chip design and to give a brief overview of the function of the circuitry involved.

The original version of this paper, for the first-generation chip, accurately describes the theory behind the continous wavelet transform and its implementation on the chip. The chip specifically addressed by that paper has been designated **WaveChip2**. A second-generation chip was designated and fabricated in January, 1992; that one has been designated **WaveChip4**. WaveChip1 was the same design as WaveChip2 but with a different aspect ratio for the layout. WaveChip3 is essentially the same as WaveChip4 but was fabricated by Zilog without a poly1/poly2 process. Also, WaveChip3 did not contain the latest version of the oscillator circuit.

The current chip is **WaveChip5**. There are three versions of this chip, one of which was submitted to Zilog but not fabricated due to delays and problems with the Zilog administration. The Zilog version will be referred to by its Zilog designation, which is **Z89c55ba**. The second version, which is a somewhat cleaned-up and expanded version of the Z89c55ba, was returned from fabrication in July, 1993, but was found to have reversed substrate contacts in several places, causing a short between power and ground; this chip was not extensively tested, but some outputs could be characterized, albeit with the chip drawing a tremendous amount of current and releasing a tremendous amount of heat. The third chip was briefly redesigned for P-well fabrication in order to meet a convenient schedule deadline; this chip will be the one presented by this paper, and will be referred to as **WaveChip5b** or simply **WaveChip5**. WaveChip5b was returned from fabrication on October 4, 1993.

The technology used to fabricate each chip is as follows:

Chip name	*Foundry*	*Min. feature size*	*Well type*	*Poly*
WaveChip2	Zilog	2.0 micron	twin-well	single
WaveChip4	Orbit	2.0 micron	P-well	double
Z89c55ba	Zilog	1.2 micron	twin-well	single
WaveChip5a	Orbit	2.0 micron	N-well	double
WaveChip5b	Orbit	2.0 micron	P-well	double

2 Wavelet Transformer Chip I/O

The current circuit design requires a total of 84 pins, as documented below. The package type for this chip will be a 84-pin PGA, a standard MOSIS package for the 4600 $\times$ 6800 micron die size.

The pinouts and their names are desribed in the Table 1. Pins are for the 84-pin PGA package, and entries are listed in clockwise order of chip pads, beginning in the upper left-hand corner on the top.

Note: This chip has been rotated 90° from the previous version; all the pin numbers below have been adjusted accordingly.

3 Chip Specifications

- Power Supply: +5V DC $\pm$5%
- Input mean value: 2.5V $\pm$1.0V
- Input p-p amplitude: 0.4V (?)
- Input frequency range: 180Hz to 12kHz (?)
- Number of filter banks: 7 + 1 test

4 Wavelet Chip block diagram

A block diagram of the Wavelet Transform chip is shown in Figure 1. The oscillator and test circuitry are not shown.

Table 1: WaveChip5b Pin List

Pin No.	*Name*	*Description*
1	A_Vdd	analog and padring Power, +5V
2	decomp_normbias	decomposition AGC output amp bias
3	Vamp3H	reference voltage to decomposition AGC, high end
4	DecompbiasH	decomposition AGC time-averaging amp, high end
5	$\overline{\text{Override3}}$	override of decomposition output AGC
6	Vamp4	bias to test section output variable resistor
7	VoutTest	Reconstructed signal output (test section)
8	Vin	signal input
9	Vinavgbias	bias for local average of signal input
10	reconavg_biasH	reconstruction input local reference, high end
11	waveavg_biasH	modulator local reference, high end
12	Resetbar	system reset signal
13	$\overline{\text{Override2}}$	override of LPF AGC
14	VtauH	Modulator LPF width control, high
15	VQH	Modulator LPF resonance control, high
16	Vamp1H	AGC reference to attenuator, high end
17	Vref	Input/Ouput voltage reference (typ. about 2.5V)
18	AttenlowbiasH	bias to attenuator AGC time-averaging amp, high end
19	CLK	External clock input
20	ExtCLK	External clock override (Input to chip is driven by CLK input)
21	A_GND	Analog and padring Ground, 0V
22	totemtest_totemout	test AGC output of inverter totem
23	totemtest_biasout	test AGC circuit feedback output
24	totemtest_capnode	average value output from AGC test
25	totemtest_vamp	reference voltage to AGC test
26	lpf_biasH	bias to LPF AGC time-averaging amp, high end
27	Override1	override of AGC on the attenuator
28	Vf	frequency-control voltage input
29	OscLowbias	bias voltage to oscillator time-average integrator
30	OscNormbias	bias voltage to oscillator high-gain amp
31	HystBias	bias voltage to oscillator hysteretic inverter
32	Mux_pbias	P-pullup bias for multiplexer OR gates (nom. 4.3V)
33	Select3	Multiplexer (I/O) select, high bit
34	Select2	Multiplexer (I/O) select
35	Select1	Multiplexer (I/O) select
36	Select0	Multiplexer (I/O) select, low bit
37	Fb_normbias	bias to matched output amps of the AGC
38	D_GND	digital Ground (isolated), 0V
39	OscTest	multiplexed output from the divide-down flip-flops
40	Abias	bias to attenuator amplifiers
41	polycap1	test capacitor poly1 connection
42	polycap2	test capacitor poly2 connection

WaveChip5 Pin List (continued)		
Pin No.	*Name*	*Description*
43	A_Vdd	analog and padring Power, +5V
44	WaveTest	muxed output from the smoothed (sinusoid) AttenTest signal
45	AttenTest	multiplexed output from the attenuated OscTest signal
46	AttenlowbiasL	bias to attenuator AGC time-averaging amp, low end
47	Vamp1L	AGC reference to attenuator, low end
48	VQL	modulator LPF resonance control, low
49	VtauL	modulator LPF width control, low
50	lpf_biasL	bias to LPF AGC time-averaging amp, low end
51	waveavg_biasL	modulator local reference, low end
52	reconavg_biasL	reconstruction input local reference, low end
53	Multbias	transamp bias for wide-range multiplier
54	Vamp5	bias to output variable resistor
55	Vout	reconstructed signal output
56	DecompbiasL	decomposition AGC time-averaging amp, low end
57	Vamp3L	reference voltage to decomposition AGC, low end
58	VgaussL	Gaussian filter width control, low end
59	WaveOut	multiplexed decomposition output
60	ResbiasTest	multiplexed average energy output
61	MultTest	output from the decomposition multiplier
62	Iin7	low-frequency reconstruction input (imaginary)
63	A_GND	analog and padring Ground, 0V
64	Rin7	low-frequency reconstruction input (real)
65	Iin6	reconstruction input (imaginary)
66	Rin6	reconstruction input (real)
67	Iin5	reconstruction input (imaginary)
68	Rin5	reconstruction input (real)
69	Iin4	reconstruction input (imaginary)
70	Rin4	reconstruction input (real)
71	Iin3	reconstruction input (imaginary)
72	Rin3	reconstruction input (real)
73	Iin2	reconstruction input (imaginary)
74	Rin2	reconstruction input (real)
75	Iin1	high-frequency reconstruction input (imaginary)
76	Rin1	high-frequency reconstruction input (real)
77	Vdrive	bias to output follower-amplifiers
78	TEST	signal to create loopback of outputs to inputs, disabling input pins
79	VgaussH	Gaussian filter width control, high end
80	D_Vdd	digital Power (isolated), +5V
81	Statres1	poly resistor test
82	Statres2	poly resistor test
83	Statres0	poly resistor test
84	Statres_common	poly resistor test

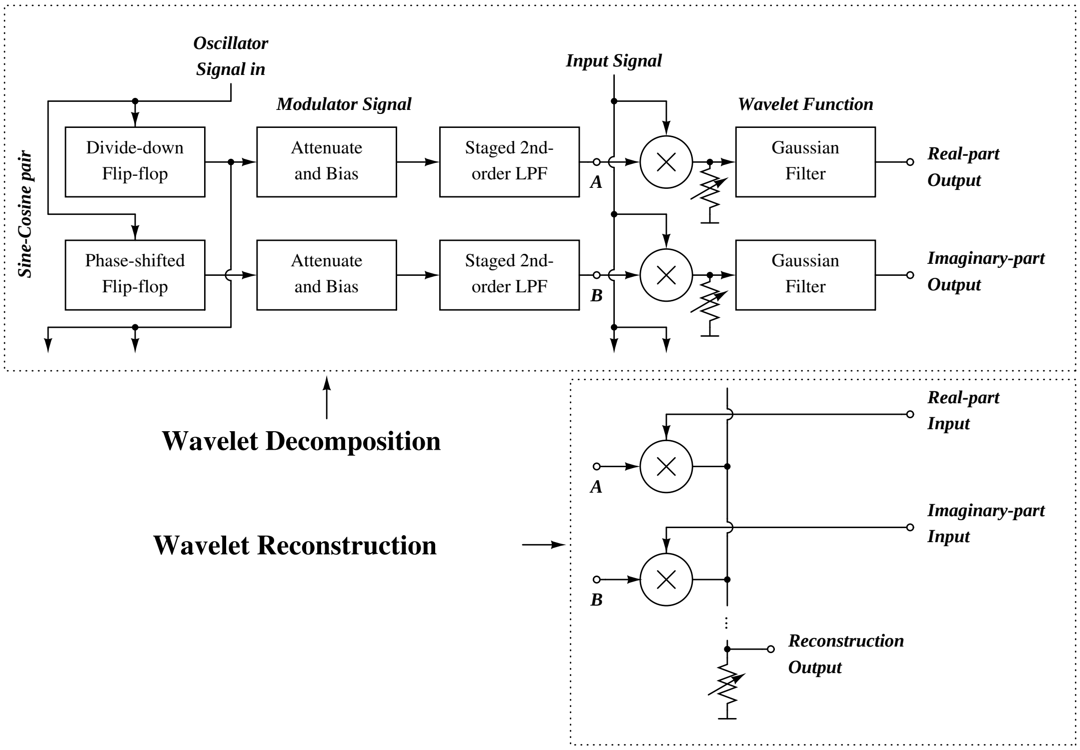

Figure 1: WaveChip5 block diagram for a single sine/cosine pair.

5 Analysis of new Analog VLSI Circuits

For the basic building blocks of the wavelet chip, see the chip specifications for **WaveChip4** and earlier designs. Only those circuits which are found on **WaveChip5** and not on earlier models (excluding the Z89c55ba), or which have undergone revision, will be presented here.

5.1 Oscillator and oscillator control logic

The voltage controlled oscillator is essentially unchanged from previous versions, except that the feedback loop on the top has been fixed to remove an unfortunate pole from the transfer function. Also the size of the capacitors was reduced to provide a higher frequency output for a given voltage input.

The digital circuitry at the bottom allows the circuit to be driven by an external clocking signal. The external signal (inverted) provides the first modulating square wave for the chip, from which all the other modulating signals are derived. Other digital circuitry (see miscellaneous circuits, below) is responsible for grounding **Hystbias** such that its output does not interfere with the driving signal. Otherwise, the driven oscillator works as usual, providing a phase-shifted version of the input at the **SinOut** output.

5.2 Flipflops

The flipflop circuit has been described in previous papers; its operation is very straightforward and it is left for the reader to verify that it does indeed cause the input square waves (which are offset in phase by 90 degrees) to be divided by half in frequency at the outputs.

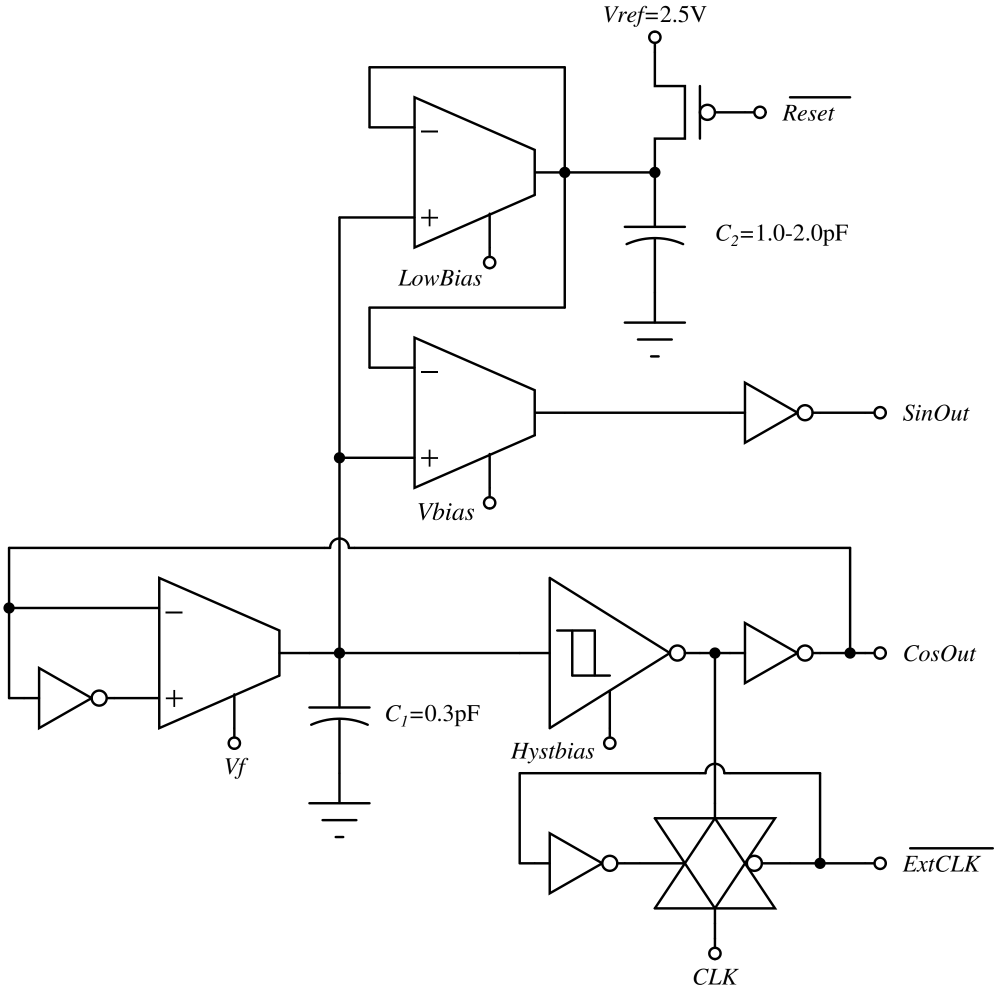

Figure 2: The low-power analog voltage-controlled oscillator.

5.3 Feedback circuit

A number of circuits were developed in order to overcome the mismatches inherent in the chip. These involved using automatic gain control in order to match the outputs of each chip slice to a desired amplitude. This circuit diagram shows the basic structure used for feedback. In general, we want to take an output signal, and based on its peak-to-peak amplitude, adjust a critical bias voltage in the circuit producing the signal such that the output is maintained at a desired level. The input circuit here is a low-current inverter, from which the output current is transformed into a voltage by the diode-connected transistor beneath the inverter CMOS pair. Since the inverter's current is greatest when the input is around 2.5V, the output voltage will "spike" whenever a zero-crossing occurs at the input. The integrator following the inverter circuit averages these spikes to produce an output voltage which is inversely related to the input peak-to-peak value. Finally, the low-gain output amplifiers are used to compare this average value to a given comparison voltage **Vamp**. Two amps are used in order (hopefully) to reduce the variance in offset voltage; also, diode-connected transistors placed beneath the input transistors reduce the gain at the output, which also helps to reduce the impact of offset voltage mismatch.

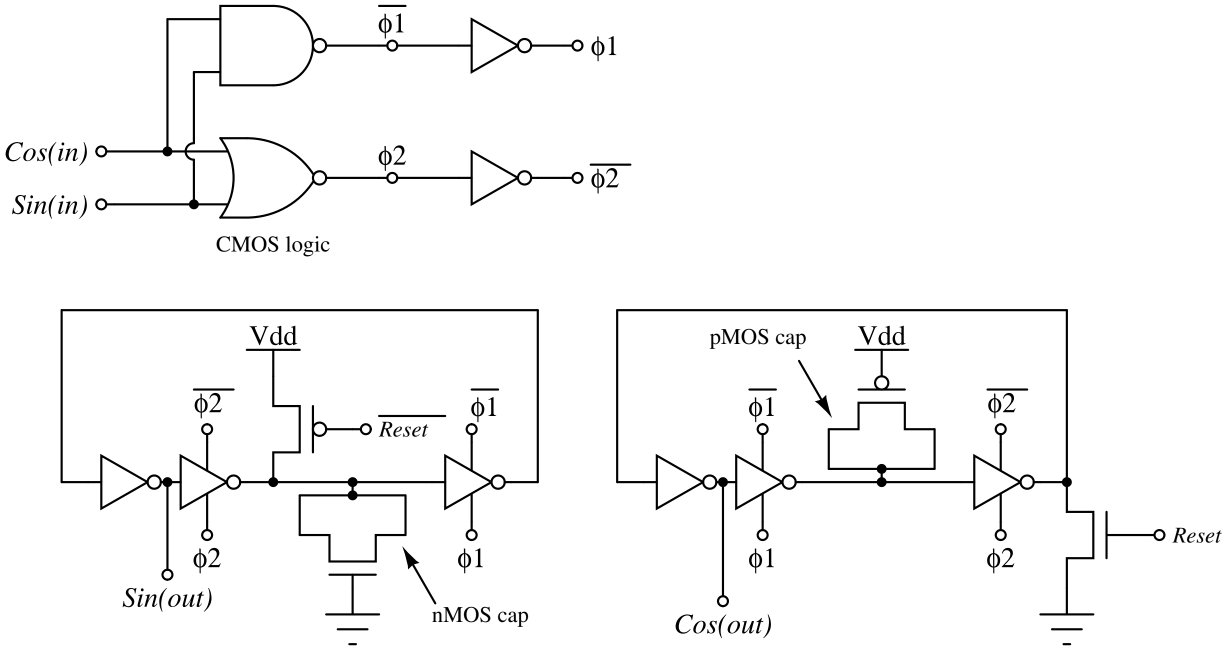

Figure 3: Oscillator divide-down flipflops.

Note: Preliminary tests on the isolated feedback section of the "hot" chip suggest that the voltage output of the feedback section works well at low frequencies but skews heavily at frequencies over about 1000Hz. If this is true of the properly-working chips as well, then the feedback mechanisms will be essentially useless at normal operating frequencies. Modifications to the design are pending.

5.4 Modulator/demodulator sections

The modulator and demodulator sections provide the same basic multiplication function as in previous chips; however, in order to minimize the effect of differences between the reference voltages of the two inputs to the multiplier, low-biased integrators have been added to provide a continuous signal mean to the multiplier. Each signal going to the multiplier has its own reference. The feedback scheme is used here in order to boost or attenuate the output signal to a constant amplitude. This is done so that the output can be sampled at a set number of bits of quantization (expected to be minimal), and the output of the feedback mechanism, which is (roughly) proportional to the average energy of the non-normalized output, contains the rest of the information about the signal. In this way, the analog circuitry further aids the digital compression mechanism at the output.

Note: In the case of the modulator shown here, the feedback system is slightly modified. The inputs to the comparator amplifiers are reversed between the positive and negative terminals, such that an increase in input peak-to-peak amplitude causes the resistor-amplifier's bias to decrease, causing the resistance to go up and therefore causing the output signal amplitude to drop.

5.5 AGC Attenuator

The attenuator acts exactly as it has previously in the case that no feedback is used; i.e., it is just a voltage averaging circuit (follower-aggregator). The application of feedback causes automatic gain

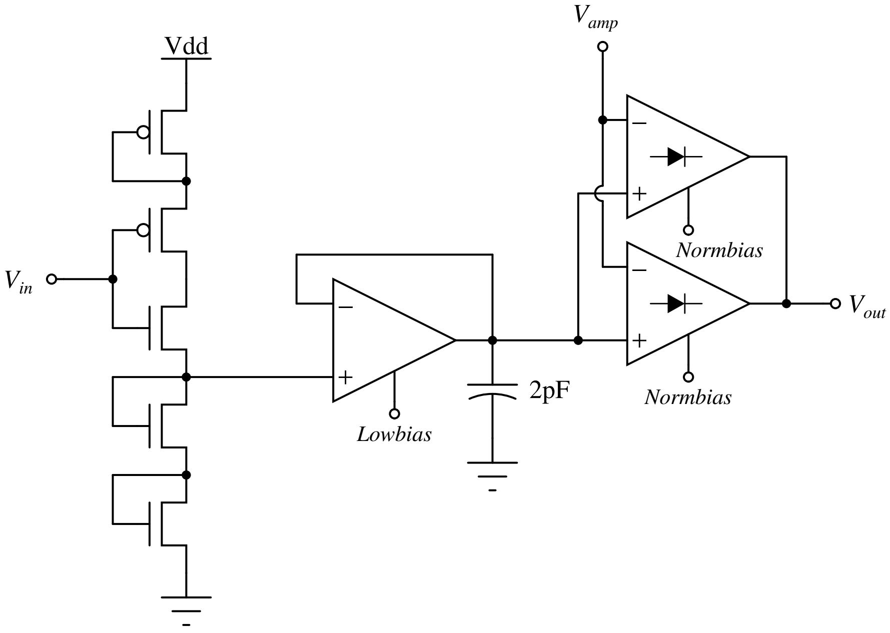

Figure 4: The basic feedback strategy for adjusting bias voltages.

control to take effect in the following manner: The input bias for the signal (which is the "weight" for the weighted average in the follower-aggregator) is increased or decreased with respect to the weight of the reference. This weight is derived from another follower-aggregator average, that of the feedback output with the bias voltage itself. In this manner, only small changes in the bias of the main signal aggregator about the mean value of **Abias** are allowed, which is necessary because small weight changes produce large output changes.

5.6 Adaptive-Q LPF

The low-pass filter of WaveChip4 was found to produce outputs which were highly non-sinusoidal regardless of the values of the **VQ** and **Vtau** biases. Assuming that this was due to a shallow cutoff slope, five cascaded LPF stages were used in WaveChip5. However, subsequent testing on the "hot" chip shows that the output nonlinearities do not go away, suggesting that some sort of slew-rate limitation is involved; i.e., that the capacitors are so large that the current output which charges them cannot force the output voltage to keep up with the input. Normally the solution is to increase the bias voltage to allow the output to provide more current, but in this case the bias voltage is restricted by the need to set a particular value of cutoff frequency. One possible solution is to vary the bias voltages from one end of the cascade to the other, but this possibility is not provided for on WaveChip5.

5.7 Output conversion

The output converters are responsible for taking the current output of the multiplier and converting it to a voltage by providing a variable resistor. The value of the resistor must be set by hand to cause the chip output to have the proper peak-to-peak swing, unless feedback is used to adjust the bias to provide a constant-energy (normalized) output as described for the modulator above. The

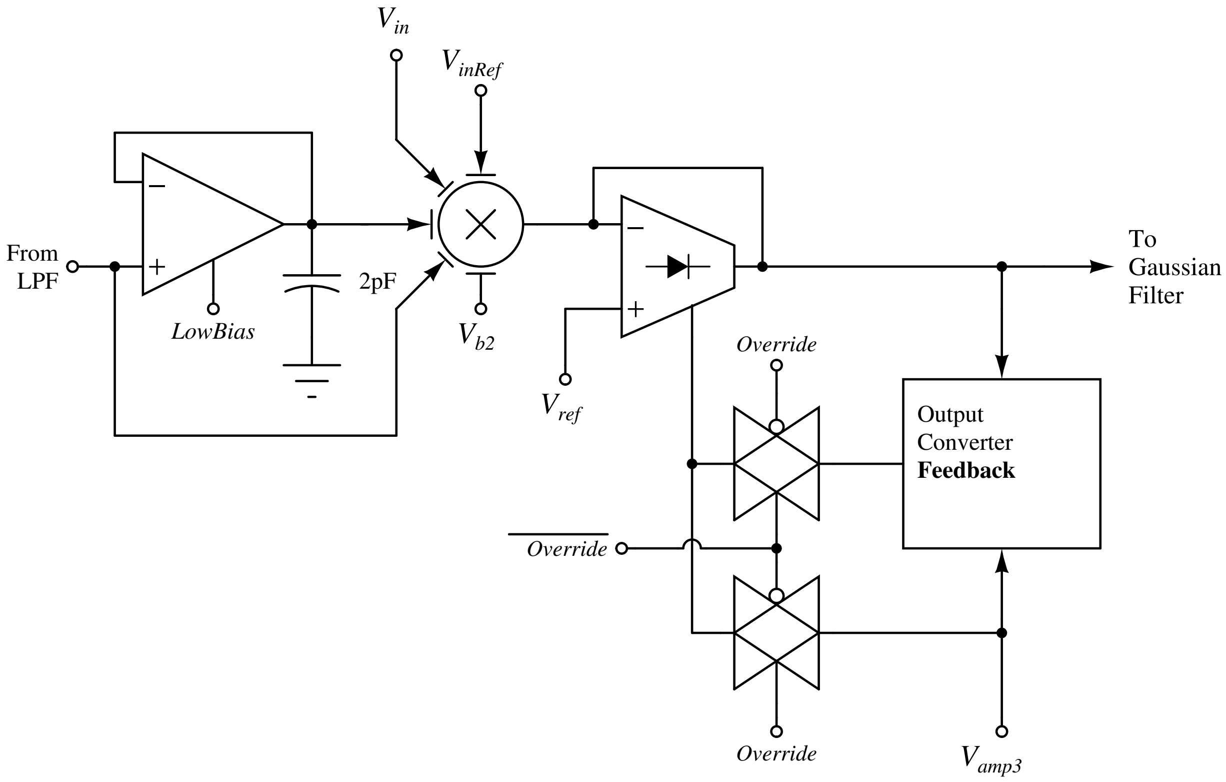

Figure 5: Modulator section.

demodulator, responsible for signal reconstruction, has all multiplier outputs tied together so that the currents add and subtract according to the basic Kirchoff laws; the final current sum is then transformed to an output voltage with a single resistor-amplifier. Each modulator (decomposition) output has its own output converter.

5.8 Low-gain, wide-range Gilbert multiplier

This circuit works essentially as described in Mead [1]. In this version, extensive use of diode-connected transistors causes each stage of the multiplier to have a reduced-gain output. This increases the linear range of the output.

Note: Nonlinearity in the output occurs whenever *either* of the inputs exceeds its linear range, so nonlinearity can show up at the output even at small output values if one of the inputs is very large and the other is very small. This is a fundamental limitation of the Gilbert multiplier.

5.9 Output multiplexer

This is the scheme which allows an increased observability of the internal workings of the chip. Two of these circuits are attached to the left and right sides of the chip, each providing three signals to the output from one of the sixteen chip slices. The left side mux provides one each of the modulating square wave (**OscOut**), the modulating sine wave, which is the LPF output (**WaveTest**), and the attenuated, biased square wave, which is the attenuator circuit output (**AttenTest**). The right side mux provides one each of the wavelet decomposition output, which is the output of the Gaussian

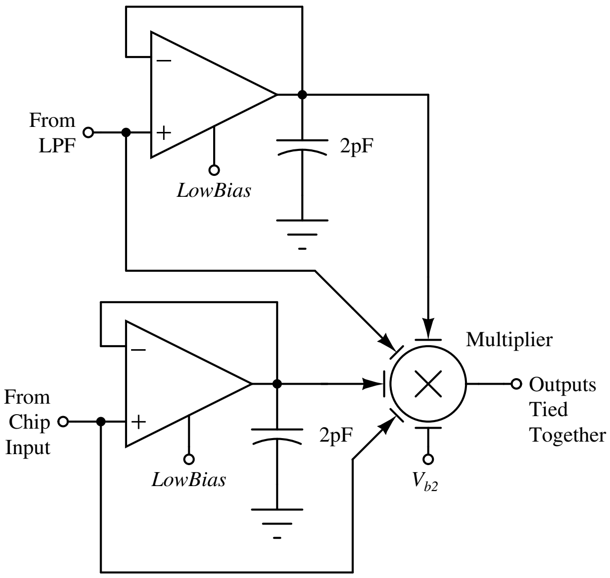

Figure 6: Demodulator section.

fileters (**WaveOut**), the decomposition multiplier output, (**MultTest**), and the average energy of the decomposition output, which is the feedback-conrolled bias of the output resistor-amplifier, (**ResBiasTest**). The lines **Select0** through **Select3** control which of the sixteen slices is selected for output. **Select0** is the low-order bit of this four-bit value.

5.10 Test mode control

This figure shows four different circuits which determine the operating mode of the chip. The two logic circuits on the left alter the meaning of the external driving signal flag **ExtCLK** and the actual driving signal itself (**CLK**), depending on the value of the reset switch **Reset**.

Of the two muxing circuits on the right, the top one is responsible for shutting off the hysteretic inverter in the oscillator whenever an external driving clock is chosen, as described in the section on the oscillator. The bottom circuit is responsible for causing the output to be redirected to the reconstruction input while disabling the input pins **Rin1, Iin1** through **Rin7, Vin7**, so that immediate reconstruction of the signal can be attained for testing purposes.

5.11 Other circuits

Some circuits have been exhaustively described in papers predating this one. These include the Gaussian filter bank, the hysteretic inverter, and the output converter (resistor-amplifier).

There are a number of follower-amplifiers which complete the inventory of circuits on this chip. They are biased at high values (**Vdrive** = 2.5V) and have large output transistors in order to provide a decently high gain for driving pads. The only exception to this scheme for viewing outputs is the **OscTest** signal, which is digital, allowing the output pad to be driven by a large inverter.

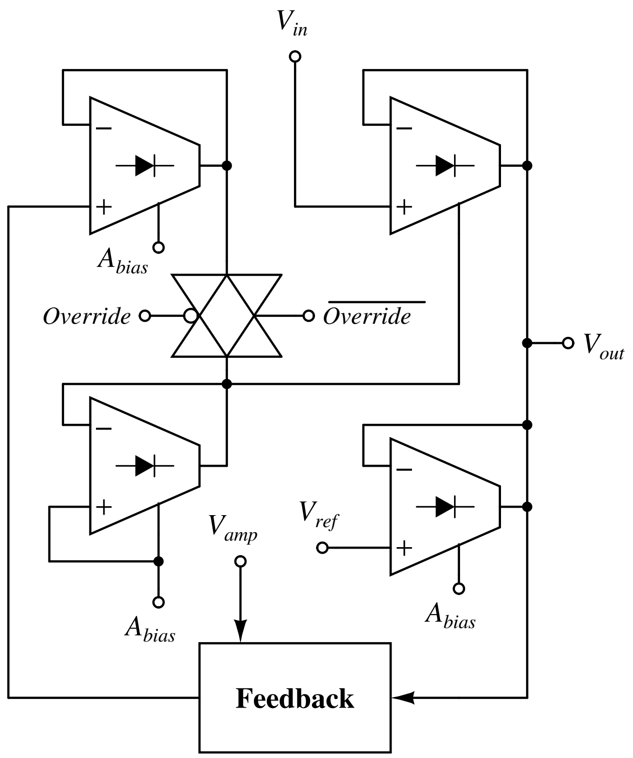

Figure 7: System for attenuating and biasing the square wave signal.

5.12 Wavelet chip slice

The block diagram of Figure 1 shows two "slices" of the wavelet chip, which make up one filter bank generating real and imaginary wavelet decomposition outputs. There are sixteen slices of this wavelet chip, each containing the logic to divide down an incoming clock (oscillator) signal, low-pass filter the oscillator to produce a smooth sine (or cosine) wave, multiply this modulating signal with two different inputs (one of them for the signal decomposition part of the transform, the other for the reconstruction half), low-pass filter the decomposition result with a gaussian-shaped function, and aggregate (average) the reconstruction result with the result from all other slices to produce a final result. Each reconstruction input is retrieved from a separate input coming from a chip pin. The decomposition output is multiplexed into a stream using a simple multiplexer with four select lines. The choice of sampling rate and time-order of the output is made off-chip. The slices of the transformer alternate between those producing sine wave modulating signals and cosine wave modulating signals (only defined by their phase relation to one another), with each pair constituting a filter bank as noted above.

In the chip pin description, the addition of **H** or **L** subscript on a signal name means the high or low endpoint value (for the high-frequency modulator output or low-frequency modulator output, respectively) for voltage on a polysilicon resistor chain.

The multiplexer select lines are defined such that when value of the vector

$$\mathtt{Select3}, \mathtt{Select2}, \mathtt{Select1}, \mathtt{Select0}$$

is equal to zero, the low-frequency imaginary slice is chosen. A value of one chooses the low-frequency real slice. Values of 14 and 15 (decimal) choose the imaginary and real high-frequency

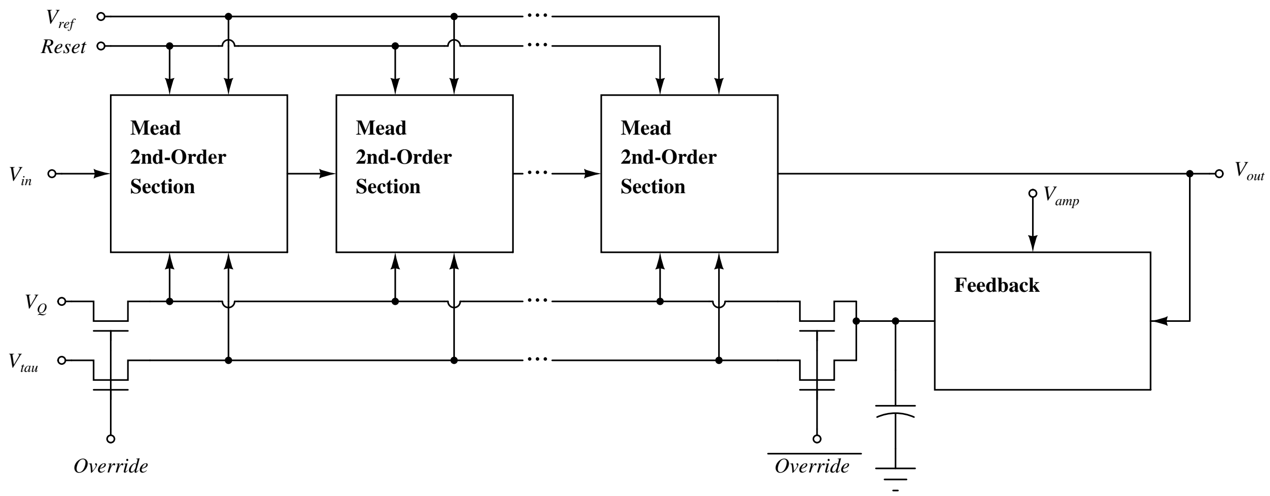

Figure 8: The adaptive-Q cascaded second-order LPF.

outputs of the test slice, respectively. Values of 12 and 13 choose the imaginary and real high-frequency outputs of the full filter bank array, respectively. Select values influence the signals which are listed in the pinout table and which are declared "multiplexed."

6 Using the Wavelet Chip

Since the theoretical results are only approximations, we expect to set the operating voltages on the chip piece by piece, according to given test procedures.

1. **Setup procedure:** The lines which must be set before beginning the test procedures are **A_Vdd** and **D_Vdd** (5.0V), **A_GND** and **D_GND** (0.0V), **Vdrive** (2.0V to 3.0V), **Vref** (2.5V), and **Mux_pbias** (4.3V). Attach **Resetbar** to a momentary toggle which defaults to 5.0V but drives 0.0V when depressed.

2. **Single slice test:** Before testing the wavelet transform as a whole, nominal values for various chip parameters (voltages) will be derived from tests to the single test slice (real and imaginary pair). Therefore, **Select1, Select2**, and **Select3** should be 5 volts, and **Select0** should be able to alternate between 0 volts and 5 volts in order to select the real or imaginary slice.

3. **No AGC test:** The wavelet chip is able to have all AGC controls disabled, in which case it acts essentially like **WaveChip4**. Since signals have been characterized through the entire signal path of a slice in **WaveChip4**, we will begin with all AGC circuits off to ensure that **WaveChip5** operates correctly in **WaveChip4** emulation mode. In order to shut off the AGC circuits, set **Override1** to 5 volts, and both $\overline{\text{Override2}}$ and $\overline{\text{Override3}}$ to 0 volts.

4. **Testing the Oscillator:** Set **OscLowbias** to 0.35V, **Hystbias** and **OscNormbias** to 0.8V, and **Vf** to a variable voltage source. Attach **OscTest** to an oscilloscope, with **Select0** at 5.0V to view the real part slice (also called the "cosine" part). Set **ExtCLK** low to disable the external clock. Set **Vf** to a value of 0.7V. This should produce a square wave on the oscilloscope. Vary **Vf1** and measure frequency at a few different points. Find the maximum and minimum frequencies at which the circuit will behave properly. Investigate the change in frequency

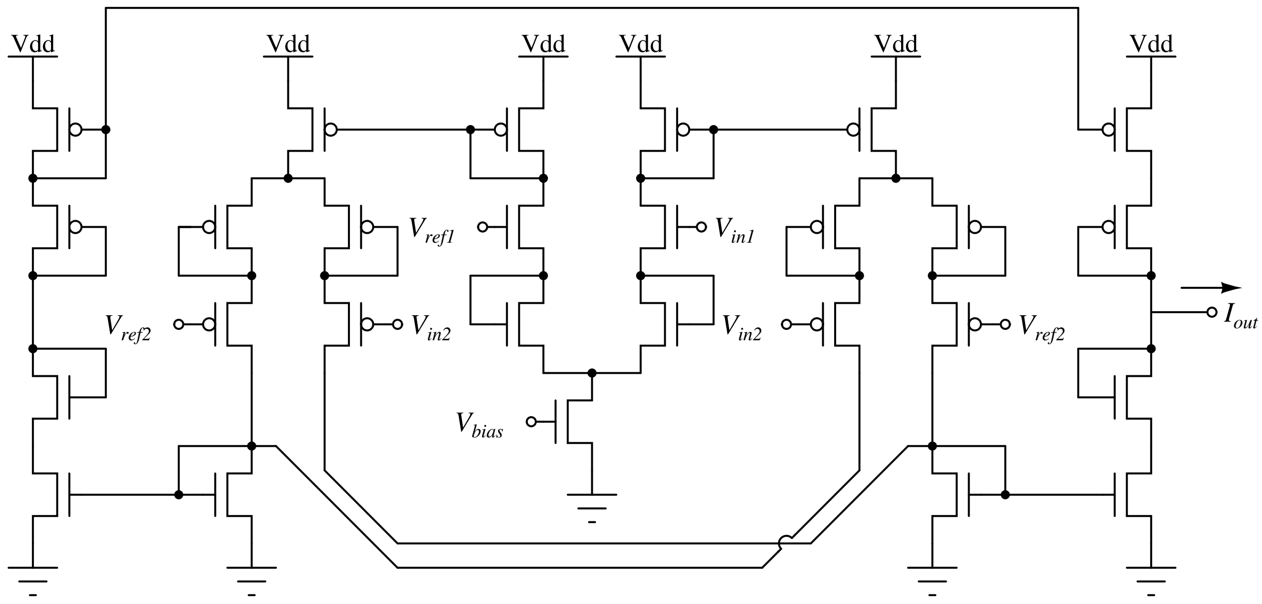

Figure 9: Circuit schematic of the wide-range multiplier.

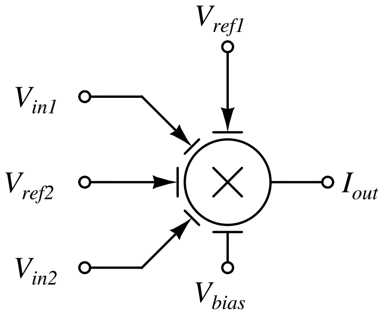

Figure 10: Symbol for the wide-range multiplier.

produced by varying the value of **Hystbias**. Set **Select1** to 0.0V and repeat the experiment for the phase-lagged output (also called the "sine" part). Investigate the change in frequency produced by varying the value of **OscNormbias** for this case. Find the best operating range for **OscLowbias**; a value which is too low will cause the output not to be able to follow slow DC changes in the oscillator. A value which is too high will distort the output, in particular changing the duty cycle of the pulse wave.

Test the reset mechanism by setting **Resetbar** low (0.0V), and then high again (5.0V). During the low state, the cosine **OscTest** output and the sine **OscTest** output should be driven high. Upon transitioning of **Resetbar** back to the high state, the cosine output should wait one-half of its normal frequency period for the applied **Vf**, and then transition low as normal. The sine output will follow lagged by a quarter-phase as normal.

5. **Testing the Flipflops:** This test will confirm the clock range over which the flipflops operate correctly. Set **ExtCLK** high, and attach input **CLK** to a function generator generating a variable-frequency square wave between 0 and 5 volts. Set **Vf** to a value which would produce the frequency (or close thereto) of the function generator as output if the oscillator

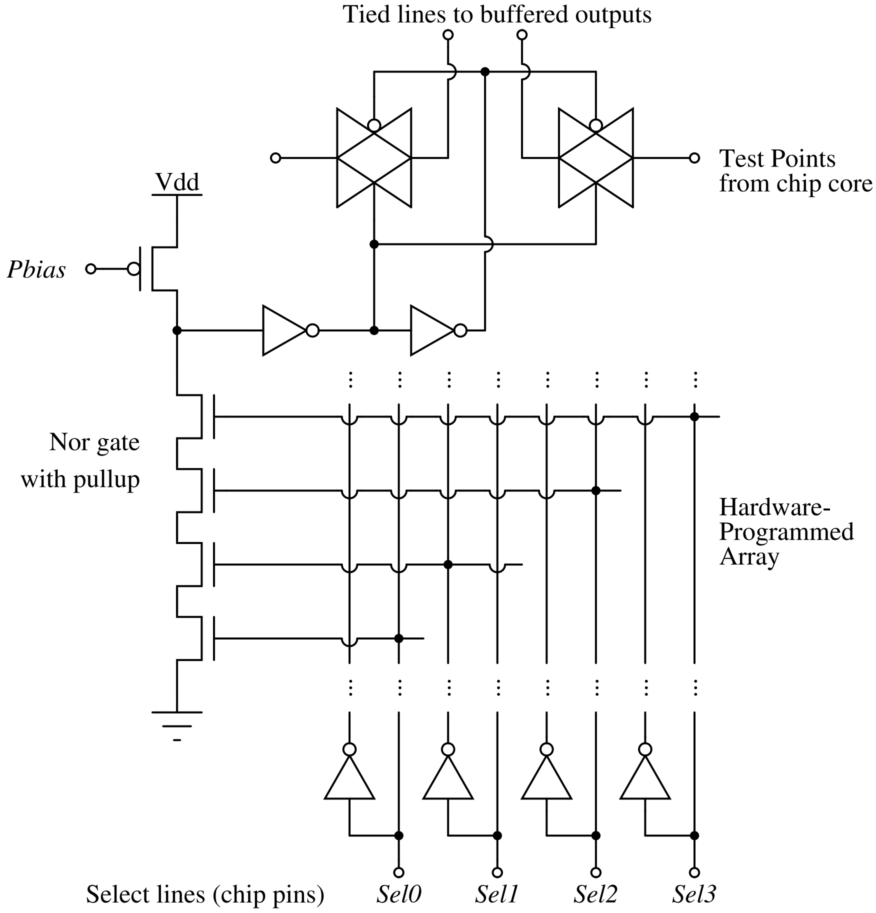

Figure 11: Multiplexing scheme for observing chip outputs.

were running in its free, non-driven mode. Display the signal **OscTest** on an oscilloscope in addition to the input function generator signal. When **Select0** is 5V **OscTest** should be the inversion of the input. When **Select0** is 0V, **OscTest** should lead the input by one-quarter of a period. Determine the frequency range of correct operation. Verify that the various values of **Select3:0** produce the correct divided-down frequency. Again, determine the proper range of **OscLowbias** over a range of frequencies.

The reset mechanism should work in a way similar to that when the oscillator is free-running. When **Resetbar** returns high, the cosine output will transition low on the next low-to-high transition of the clock.

6. **Testing the Modulator Attenuator (without feedback):** Set **Abias** to 0.8V. Set the external or internal clock rate to a value at which the wavelet chip will be expected to operate. Examine the value **AttenTest** for all slices of the chip. Compute the mean and variance for the amplitudes over the sixteen slices. Is there an amplitude dependence on the value of **Vref**? On the value of **Abias**? If so, what are these dependencies? The main consideration here is the variation in amplitude of the attenuated signal over different slices.

7. **Testing the Modulator LPF:** Set **VtauH** to about 0.61V and **VQH** to about 0.60V. Leave **VtauL** and **VQL** disconnected. Attach the signal **WaveTest** to an oscilloscope. Adjust the

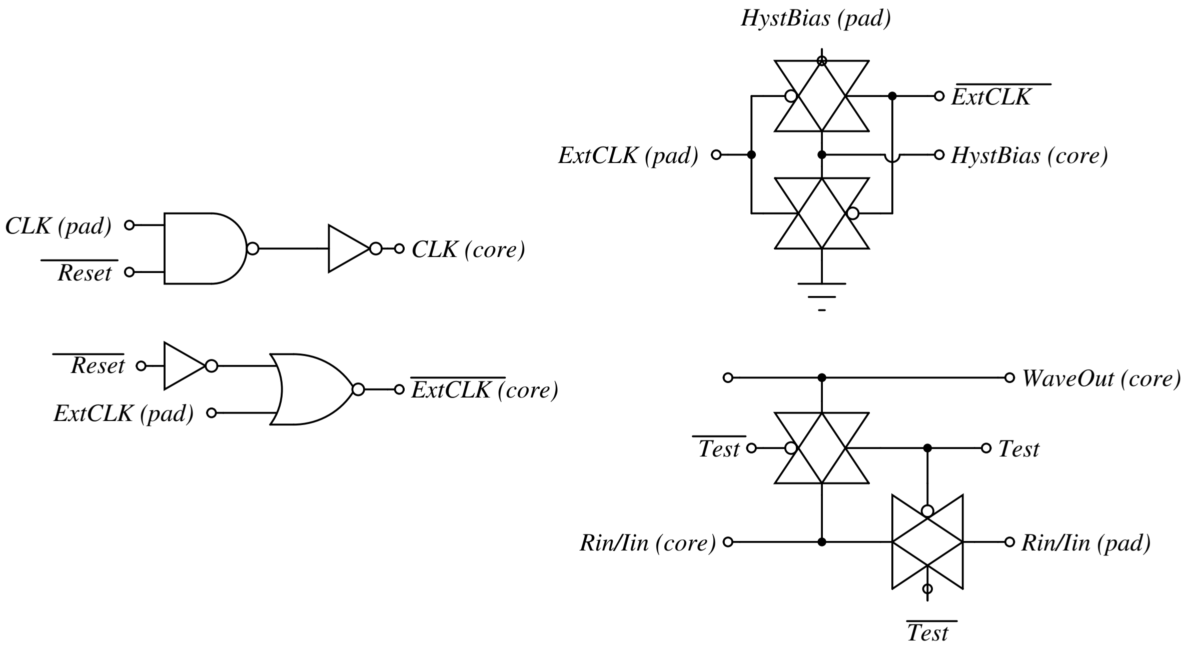

Figure 12: Miscellaneous logical functions on WaveChip5.

values of **VtauH** and **VQH** until the output best matches a sinusoid. Generally, **VtauH** should remain about 0.01V higher than **VQH**. The adaptive-Q mechanism, when on, always uses equal values for **Vtau** and **VQ**, so also determine what the optimal value is at each frequency when these voltages are equal. Is a clean sinusoid available in all cases? What are the frequency bounds for a clean output?

Try to modify the gain using **Abias** (and also **VQH** and **VtauH** if necessary) to set the peak-to-peak amplitude of **WaveTest** for the test section to about 0.4V. Repeat the test for an oscillator rate of 1/64 of the first test. When done, set **VtauH** and **VQH** to the values determined from the first test, and **VtauL** and **VQL** to the values determined from the second test.

8. **Testing the Modulator Multiplier:** Initially set pins **MultBias** and **Vamp3H** to 0.8V each. Set **Vinavgbias** and **Waveavg_biasH** to about 0.4V each. Leave **Vamp3L** and **Waveavg_biasL** disconnected. All other pins should remain as they have been set from the previous tests. This test is important to keep the output of the multiplier from overflowing. Set pin **Vin** to 2.5V (or attach to pin **Vref**), and the pin **MultTest** to an oscilloscope. The output **MultTest** should be nearly constant and equal to 2.5V. Any offset in the multiplier and time-averaging circuits will cause some of the input modulating signal to couple through to the output. Determine this offset for each slice by measuring the amplitude of the **MultTest** signal. Also determine the value of **Waveavg_biasH** which minimizes this effect for each frequency. When these values are determined, set **Waveavg_biasL** to a value appropriate for the low frequency end of the transformer.

   Now, generate a sine wave at the input **Vin**, centered at 2.5V (**Vref**), and having a peak-to-peak amplitude of 0.4V. Using the results found above for the best **Waveavg_biasH** *vs.* frequency, set **Vinavgbias** to a value consistent with the input frequency. The output **MultTest** should be a signal containing the sum and difference of the function generator sinusoid and the **CLK** input (or the output from the voltage-controlled oscillator, if that is being used instead). Adjust **Vamp3H** until the multiplier output is well-behaved, and approximately 0.4V peak-to-peak. Repeat this experiment for the other sections, then set **Vamp3L** at a voltage consistent with the required voltage for the low frequency end of the filter bank, if it is any different. Otherwise, connect the pin directly to **Vamp3H**.

9. **Testing the Gaussian Filter:** Set **VgaussH** to 0.4V, and do not connect **VgaussL**. The output of **WaveOut** should now reflect the value at the output of the first gaussian filter. Adjust **VgaussH** until the high frequency part of the signal is attenuated and only the low frequency part remains.

   For several values of **VgaussH** between about 0.4V and 0.7V, measure the amplitude of **WaveOut** *vs.* the frequency of the output for a sweep of frequencies to **Vin**. When done, find the -3dB cutoff frequency for each. Set **VgaussH** to a value appropriate for the normal operating frequency of **Vin**, and **VgaussL** to a value appropreate for a frequency 1/64 times that. Finally, test each filter bank to check that the output amplitude peaks at the center frequency of each band and has a bandwidth appropriate for each channel. Plot the individual frequency responses of each channel and the overall frequency response of the system (the sum of the frequency responses for each channel).

10. **Testing the single-channel Recomposition Output:** Set the **Test** line low (0.0V) in order to disconnect the decomposition outputs from the reconstruction inputs. Initially, we will confirm reconstruction for the single test channel (real and imaginary parts) only, so the output to look at will be **VoutTest** and the controlling bias for the output converter will be **Vamp4**, which should initially be set to about 0.8V. Set **Reconavg_biasH** to about 0.4V, and leave **Reconavg_biasL** disconnected.

    Generate a constant input to **Rin1** and **Iin1**. The reconstruction signal should be constant at about 2.5V. If one of the inputs is changed instantaneously with a step voltage, the output **VoutTest** should briefly output a sinusoid at the center frequency of the test section, which will die off to a constant in a time span determined by the value of **Reconavg_biasH**. Now present a sinusoid signal to **Rin1** and **Iin1**, preferably 90° out of phase if possible, and at about 0.4V p-p amplitude. Adjust **Vamp4** to make the output have the highest possible gain without distortion. As the input frequency gets farther from zero, the reconstruction output frequency should move from the center frequency of the section. If the phase of **Rin1** leads **Iin1**, then the frequency should go up. If the phase of **Rin1** lags **Iin1**, then the frequency should go down.

    Now set the value **Test** to 5.0V, to enable local loopback from the decomposition outputs to the reconstruction inputs. Check that the system is able to reconstruct any signal from **Vin** with an amplitude peak at the center frequency of the band and attenuating to either side according to the bandwidth determined by **VgaussH**.

    Repeat the above experiments for the system as a whole, using **Vamp5** in place of **Vamp4** and **Vout** in place of **VoutTest**. All inputs **Rin1:7** and **Iin1:7** will be used for inputs; test one section at a time by setting all other input channels to a constant voltage value such as **Vref**.

From results of the previous two fabricated wavelet chips, it is expected that the variance in output amplitude of the square wave from the attenuator section and the mismatch of filter sections in the LPF will prevent a clean sinusoid modulating signal from being produced for every channel of the wavelet transform. In order to resolve this problem, two AGC feedback circuits have been added to the system. Their operation is outlined below.

1. **The Feedback test circuit:** One corner of the chip is devoted to a single sample of the AGC feedback circuit used in the chip. First, attach **CLK** to a variable voltage supply. Adjust the voltage until the value of **totemtest_totemout** reaches a maximum. The value of **CLK** will then be the optimal reference voltage for operating the system. Set **Vref** to this value. The test circuit can also be used to find the best values for the time-integrator amplifier bias, the output amplifier bias, and the output amplifier reference. **Lpf_biasH** is the time-integrator amplifier bias to the test circuit, **Oscnormbias** is the output amplifier bias, and **totemtest_vamp** is the output amplifier reference voltage. Change the clock to a square wave input with a p-p amplitude comparable to the output of **AttenTest** measured earlier. Adjust the value of **Lpf_biasH** until the output at **totemtest_capnode** has a minimum of ripple. Repeat for various frequencies of the input. Set **Oscnormbias** to about 0.8V, and set **totemtest_vamp** to the DC value of **totemtest_capnode**. Observe the output at **totemtest_biasout**. Adjust all the bias and reference voltages until the output is relatively stable around 0.4 to 1.0V. The two bias voltages and reference voltage will be the optimal values to present to the wavelet transformer circuit. Make a table of these optimal values over a range of frequencies.

2. **Testing the Attenuator AGC:** Using the above measured values, set **AttenlowbiasH**, Fb_normbias, and **Vamp1H**, to the optimal values for the given oscillator frequency. Set **Override1** to 0.0V. Observe the output **AttenTest** for the test slice. Readjust **Vamp1H** in order to control the output amplitude; set it to a value which makes the output approximately 0.4V p-p. Next, set **Vamp1L** and **AttenlowbiasL** to values appropriate for the low frequency slice of the wavelet transformer. Observe the output of the last (low frequency) slice and adjust **Vamp1L** to make that output approximately 0.4V p-p. Now measure the variance of the p-p levels of all the **AttenTest** outputs, which should ideally be the same.

3. **Testing the LPF AGC:** Automatic Gain Control for the Lowpass Filter uses the same circuit as does the Attenuator AGC. Therefore set **lpf_biasH** to the same value as **AttenlowbiasH**, and set **VtauH** (also called Vamp2H, becuase it serves a dual purpose) to the value of **Vamp1H**. **VQL** and **VQH** may be disconnected. Disconnect **VtauL** (which is also Vamp2L). Set $\overline{\text{Override2}}$ to 5.0V. Repeat the same procedure as above in order to get the output **WaveTest** for the test slice to be approximately 0.4V p-p. The resulting sine wave should be clean and undistorted. Also repeat the above procedure for the rest of the wavelet chip channels. Provided that the modulation signal is preferred to that using no AGC circuitry, the procedures for characterizing a signal through the chip should be repeated.

One final check is for the value of the poly1-poly2 capacitors. The capacitance value between pins **polycap1** and **polycap2** should nominally be 27 pF + the capacitance of the pads, which should not be more than about 1.5 pF each. Measure this value and its variance over the set of chips.

References

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