An Analog Wavelet Chip for Speech Compression

Chip Specifications

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Abstract

This paper describes the theory and implementation in CMOS technology of a circuit which performs analog wavelet decompositions of a one-dimensional (e.g., sound) input. The circuit is based on the Analog VLSI techniques described by Carver Mead in *Analog VLSI and Neural Systems* [1]. The analog wavelet outputs are the output of a logarithmically scaled set of bandpass filters; each band is sampled at a rate proportional to the Nyquist rate of the highest frequency content of that band. The result is a matrix of discrete points describing the input signal as a function of both frequency and time. The filter function of each band is gaussian shaped in order to best resolve the uncertainty relation between time and frequency at each sampled point. This chip has been designed by Tim Edwards under the direction of Michael Godfrey, and fabricated by Zilog Corporation of Campbell, California. Zilog provided the funding for this project.

1 Overview

This paper describes the Analog Wavelet Transform chip, a CMOS subthreshold circuit design intended for use in an experimental speech compression system. This chip was built as an alternative to using a computer or DSP system to perform the same calculations; the advantages of this approach are reduced size and power consumption. The resulting analog implementation is inflexible in terms of ability to reprogram the function performed, and requires dealing with the problem of temperature sensitivity, variable process parameters, and noise injection throughout the circuit. However, we believe that the circuit will be effective for speech signals and will be smaller and cheaper than the digital alternatives.

The Wavelet transform performed by the chip is an analog filtering function and is similar to what is known as the Gabor spectrogram (and is not to be confused with the Discrete Wavelet Transform)[2], which divides a signal into a set of frequency bands (in this case, six), often on a logarithmic scale, using a gaussian-shaped filter as the bandpass function. We have used complex demodulation so that the center frequency of each filter band is zero. Two outputs for each filter band preserve phase information about the signal in order to provide the ability to reconstruct the signal from its decomposed outputs. The total combined bandwith of the outputs is approximately equal to the bandwidth of the original signal.

The expected completion date for the fabrication of the chip at Zilog is November 1, 1992, and the system implementation of the speech compression system should be completed by the end of the year.

2 Complex Demodulation

The Wavelet function must act as a log-scale adjustable bandwidth bandpass filter on the input signal. In order to simplify the process of designing bandpass filters of adjustible center frequency and width, we use a demodulation process to convert the center frequency of each filter band to zero before filtering [4]. In this manner, each required bandpass filter is reduced to two simple lowpass filters. The (re)modulation process is similar to the demodulation, so the decomposition and reconstruction parts of the chip are nearly duplicates of the same circuit. The whole process is known as *complex demodulation.* This method is described below.

The input function is designated by $f_{\text{in}}(t)$. In order to demodulate it with respect to some given frequency ω_c (one of the center frequencies of the wavelet decomposition), then we use the following multiplication:

$$f_{\text{out}}(t) = 2\text{LPF}(f_{\text{in}}(t)(\cos\omega_c t + i\sin\omega_c t)).$$

Since the low-pass filter $\text{LPF}(\cdot)$ is assumed to be real, and $f_{\text{in}}(t)$ is real, then the output $f_{\text{out}}(t)$ must necessarily be complex, and can be represented by

$$f_{\text{out}}(t) \equiv f_{\text{real}}(t) + i f_{\text{imag}}(t).$$

Therefore,

$$f_{\text{real}}(t) = 2\text{LPF}(f_{\text{in}}(t)\cos\omega_c t)$$

and

$$f_{\text{imag}}(t) = 2\text{LPF}(f_{\text{in}}(t)\sin\omega_c t).$$

In other words, the "real" and "imaginary" parts are both results which are easily obtained by multiplying the input by two sinusoids which are 90° out of phase with each other.

The need for the factor of 2 can be seen by the following example: If $f_{\text{in}}(t) = \sin\omega_1 t$, then using the identities for $\cos(\alpha+\beta)$ and $\cos(\alpha-\beta)$, it can be shown that

$$\sin(\omega_1 t)\sin(\omega_c t) = \frac{1}{2}(\cos(\omega_1 t - \omega_c t) - \cos(\omega_1 t + \omega_c t)).$$

Here it is easily seen that each part (sine and cosine) of the demodulation process produces a new signal which contains the sum and the difference of the original and "carrier" frequencies. Since we are demodulating the carrier frequency down to zero, we are interested only in the difference, so we low-pass filter the function to get rid of the part containing the sum of the two frequencies. Since we have destroyed half of the energy of the signal by the filtering process, we must multiply the result by two. The remaining difference does not differentiate between signals on one side or the other of ω_c (e.g., $\cos(\omega_1 t - \omega_c t) = \cos(\omega_c t - \omega_1 t)$). However, this information is preserved in the relationship between $f_{\text{real}}(t)$ and $f_{\text{imag}}(t)$, as shown by the exact reconstruction below.

In order to remodulate the signal back to its original frequency, we perform the following multiplication:

$$\hat{f}_{\text{in}}(t) = f_{\text{out}}(t)(\cos\omega_c t - i\sin\omega_c t).$$

This is the same function as the demodulation except for the change in sign. We multiply out the real and imaginary parts of this equation to get a purely real result, which is the (exact) reconstruction of the original input:

$$\hat{f}_{\text{in}}(t) = f_{\text{real}}(t)\cos\omega_c t + f_{\text{imag}}(t)\sin\omega_c t.$$

Here the signs have worked out such that the remodulating sinusoids have exactly the same phase relation as the demodulating sinusoids. Note that no low-pass filter is needed for reconstruction.

3 Wavelet Function and outputs

The design of the circuit which approximates a gaussian filter (as described by Grossman [2]) is based on a probability argument. Because the signals are first demodulated, it is only necessary to create one half of a gaussian, centered around zero. When the signals are remodulated to their respective center frequencies, this low-pass filter will behave as if it were reflected symmetrically across the modulation frequency, becoming a band-pass filter with gaussian characteristics. The following transfer function describes the filter we designed:

$$H(s) = \frac{V_{\text{out}}}{V_{\text{in}}} = \left(\frac{1}{\tau s + 1}\right)^n$$

This filter consists of a cascade of n follower-integrator sections in series. Although the above expression converges to a delta function in the limit $n \to \infty$ for constant τ, it can also be shown that when τ is replaced by an expression which maintains constant bandwidth, the transfer function approaches a gaussian function as $n \to \infty$:

$$H(s) = \frac{V_{\text{out}}}{V_{\text{in}}} \approx e^{-\frac{\omega^2}{2\sigma^2}}$$

A proof of this equation can be found in Siebert [5], and shows that the gaussian shape is an example of the central limit theorem; in other words, it is a result of the use of cascaded stages and is relatively independent of the shape of the filter.

Due to considerations of signal-to-noise ratio, and the ability to generate a given constant τ from a voltage applied to the follower-integrators, we chose a cascade order of five sections. For $n = 5$ the relationship between τ and σ is:

$$\sigma = \frac{1}{\tau}(.5372).$$

The center frequencies of the filters in the filter bank are spaced on a $\log_2$ scale. Given the speech-quality frequency constraints on the input signal, we decided that six outputs would be sufficient, giving typical center frequencies of 9kHz, 4.5kHz, 2.25kHz, 1.125kHz, 562.5Hz, and 281.25Hz. The center frequency of the highest-frequency filter is generated by an oscillator circuit, which can either generate its own sinusoid with a voltage-controlled frequency, of alternately generate a sinusoid from an externally applied clock signal. The center frequencies of the rest of the filters are determined by dividing down the oscillator appropriately. The externally applied clock signal is most desirable for the speech compression application, since the frequency bands will be fixed and the external clock is less prone to drift due to temperature change. The onboard oscillator is useful for effects such as reconstructing a signal at a higher or lower overall frequency from that at which it was recorded.

The bandwidth of each gaussian filter is automatically set with respect to the others with the exception of the first and last filters, which have widths adjustable using two control voltages. In terms of the transfer function given above for the gaussian lowpass filter, the parameters τ of the highest- and lowest-frequency filters is fixed by these control inputs. τ and the effective center frequency of each filter band vary logarithmically across the bank. τ should be calculated to assure that the width of each gaussian increases proportionally with the value of the center frequency. Gaussians should overlap those in adjacent bands to minimize the notches in the overall frequency domain transfer function.

The filter transfer function for the gaussians across the entire frequency range is shown in Figure 1.

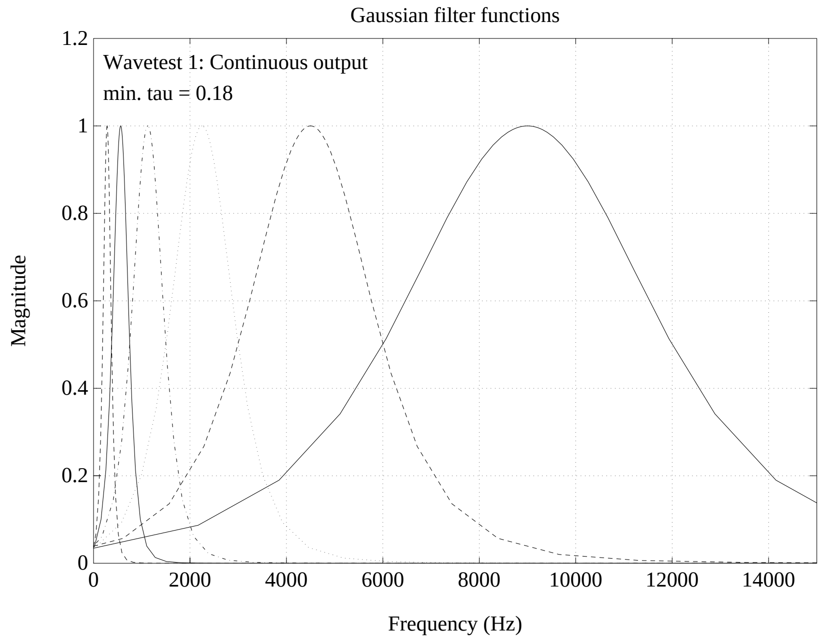

Figure 1: Gaussian filter functions.

4 Frequency-Time Description

If the outputs of the wavelet transform are used in their continuous form, then the transform always produces redundant information. The most efficient (non-redundant) description of the signal is achieved by sampling the wavelet outputs.

Figure 2 shows how proper sampling of the outputs of the chip creates a set of points which best describe the input signal as a function of both time and frequency. If the filter bands are sampled in the binary-tree fashion shown, then each band can be sampled at a rate proportional to its bandwidth, and all of the samples can be time-division multiplexed into an output stream.

Each rectangle in the time-frequency plane has an equal area; this is the area over which the filter calculation is made at the time and in the filter band that the sample was taken. The bottom part of the figure shows the gaussian filters which produce each sampled value.

5 Wavelet Transformer Chip I/O

The current circuit design requires a total of 54 pins, as documented below. The package type for this chip will be a 68-pin PLCC package.

The pinouts and their names are desribed in the Table 1. Pins are for the 68-pin PLCC package, and entries are listed in clockwise order of chip pads, beginning in the upper left-hand corner on the top.

WaveChip2 Pin List			
Pin No.	*Name*	*Alt. Name*	*Description*
1, 3, 5	ReconI[3:1]	ReconI3, etc.	Reconstruction inputs (imaginary)
2, 4, 6	ReconR[4:6]	ReconR4, etc.	Reconstruction inputs (real)
7	V_{bHI}	Vdrive	Bias to output follower-amplifiers
8	V_{refR}	VrefR	Reference voltage, reconstruction ($\approx$ 2.5V)
9	V_{b3R}	Vb3R	Transamp bias for resistor (reconstruction)
10	V_{in}	Vin	Signal input
14	GND	GND	Ground, 0V
15	V_{b3D}	Vb3D	Transamp bias for resistor (decomposition)
16	V_{refD}	VrefD	Reference voltage, decomposition ($\approx$ 2.5V)
17	V_{b1}	Vb1	Transamp bias for attenuator
18	CLKout	CLKout	Output from the last divide-down flipflop
19	$V_{\tau\mathrm{L}}$	VtauL	Modulator LPF width control, low
20	V_{QL}	VQL	Modulator LPF resonance control, low
21	V_{b2}	Vb2	Transamp bias for wide-range multiplier
26	τ_{L}	VgaussL	Gaussian width control, low end
27, 29, ...37	DecompI[6:1]	DecompI6, etc.	Decomposition outputs (imaginary)
28, 30, ...38	DecompR[6:1]	DecompR6, etc.	Decomposition outputs (real)
39	$\overline{\mathrm{TEST}}$	TESTbar	Signal to create loopback of outputs to inputs, disabling the pins
40	τ_{H}	VgaussH	Gaussian width control, high end
41	V_{out}	Vout	Reconstructed signal output
42	CosOscTest	CosOscTest	Output from the first divide-down flipflop
43	MultTest	MultTest	Output from the first signal multiplier
44	V_{QH}	VQH	Modulator LPF resonance control, high
49	CosWaveTest	CosWaveTest	Output from the smoothed (sinusoid) CosOscTest signal
50	$V_{\tau\mathrm{H}}$	VtauH	Modulator LPF width control, high
51	SineOscTest	SineOscTest	Output from the first divide-down, phase shifting circuit
52	DblOscTest	DblOscTest	Direct voltage output from the double oscillator
53	ExtCLK	ExtCLK	External clock override (Input to chip becomes signal from CLK instead of the voltage-controlled oscillator output)
54	CLK	CLK	External clock input
55	V_{f}	Vf	Frequency-control voltage input
56	Vdd	VDD	Power, +5V
60	OscVbias	Vb0	Transconductance amplifier (transamp) bias voltage
61	OscPbias	pbias	Transamp p-transistor bias voltage ($\approx$ 5V - V_{b})
62	V_{bSum}	Vbsum	Bias to summation follower-amplifiers
63, 65, 67	ReconI[6:4]	ReconI6, etc.	Reconstruction inputs (imaginary)
64, 66, 68	ReconR[1:3]	ReconR1, etc.	Reconstruction inputs (real)

Table 1: Pin list for the WaveChip 68-pin PLCC package.

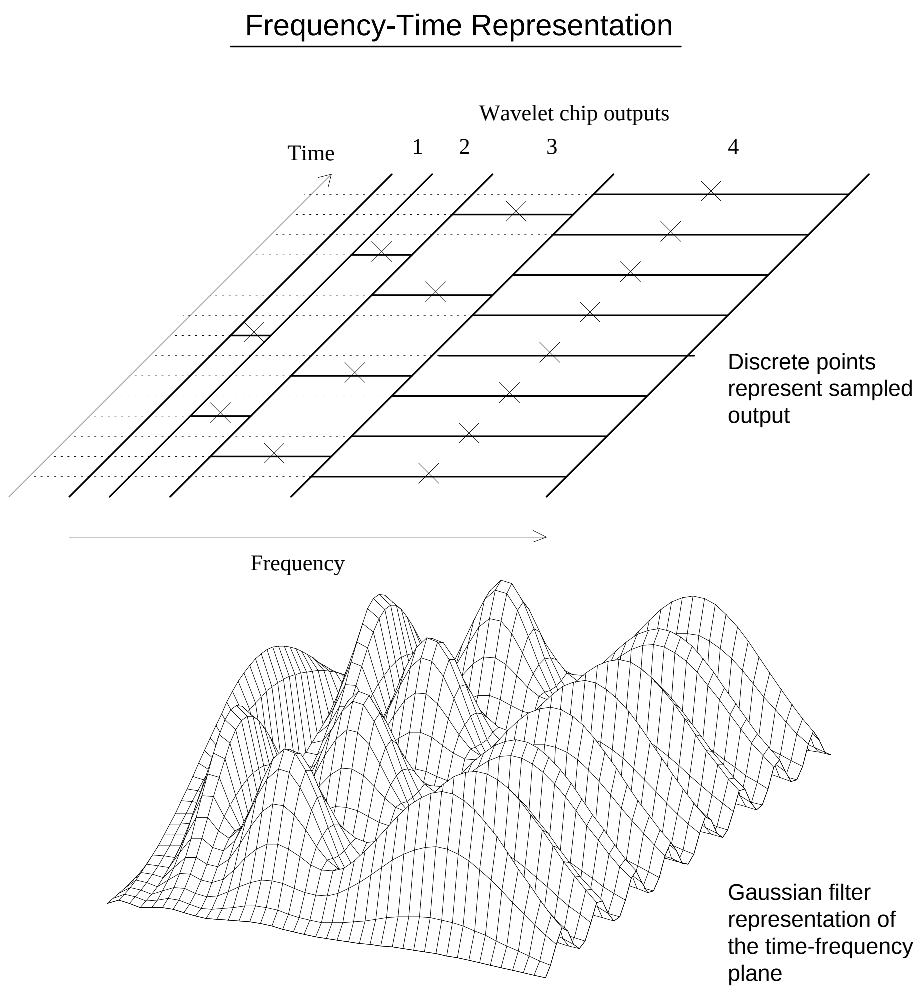

Figure 2: Output sampling and frequency-time representation of the input.

6 Chip Specifications

- Power Supply: +5V DC ±5%
- Input mean value: 2.5V ±1.0V
- Input p-p amplitude: 0.4V
- Input frequency range: 180Hz to 12kHz
- Number of output channels: 12 (6 pairs)
- Center frequencies of outputs: Adjustible (see above)
- Wavelet function: Gaussian bandpass filter
- Silicon area: 7.0 $\times 10^5 \mu m^2$ in Zilog Z-40 process
(1.96 $\times 10^6 \mu m^2$ in Zilog Z-20 2.0 micron process)
- Input and Output SNR: To be determined
- Chip package: 68-pin PLCC

7 Wavelet Chip block diagram

A block diagram of the Wavelet Transform chip is shown in Figure 3. The oscillator and test circuitry is not shown.

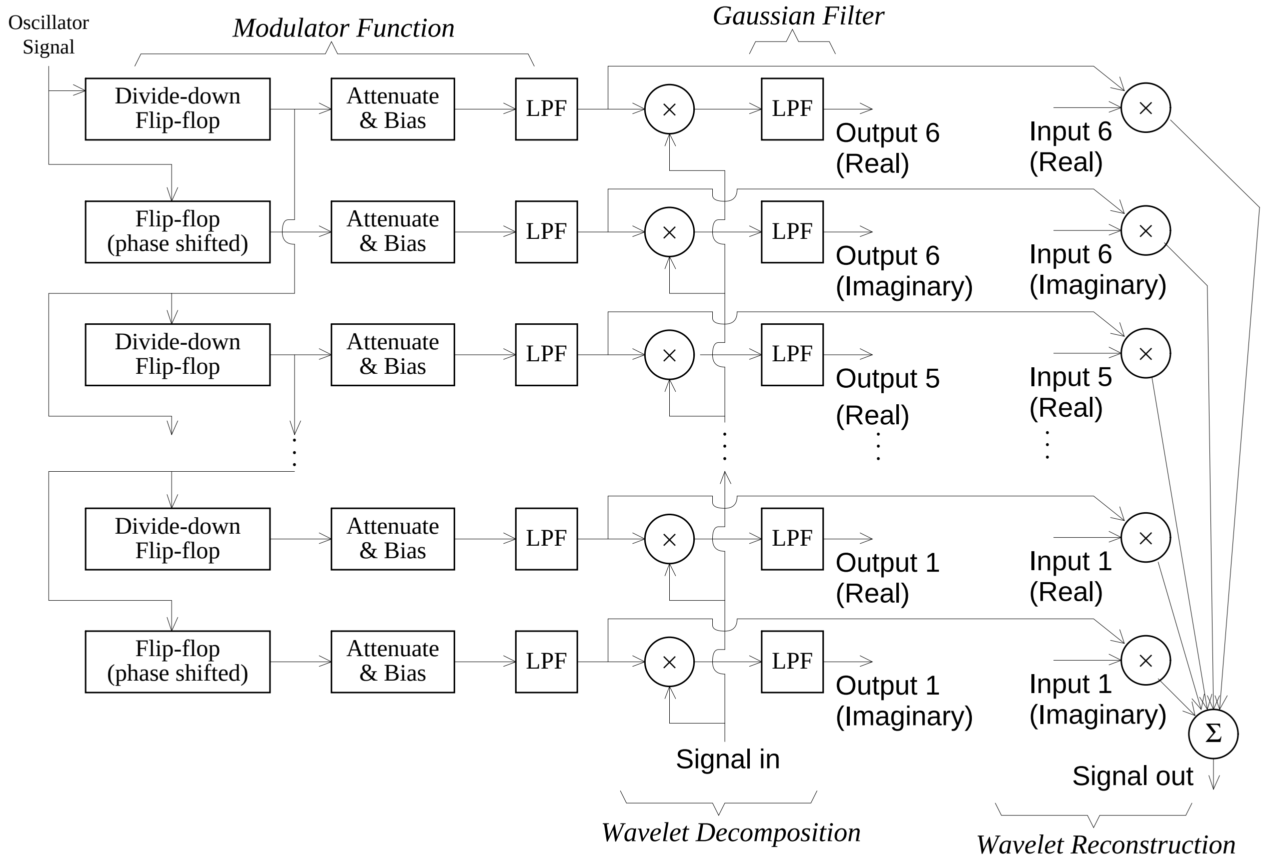

Figure 3: Wavelet Transform Chip block diagram.

8 Analysis of Analog VLSI Circuits

Figures 4 through 16 show the building-block circuits of the wavelet transform. A detailed analysis of some of the basic circuits can be found in Mead [1]. These include the wide-range transconductance amplifier (Figure 4), the wide-range Gilbert multiplier (Figure 9), the second-order section (Figure 10), and the follower-aggregator (Figure 11). These can be found on pages 67–80, 90–96, 179–192, and 105–107, respectively, of *Analog VLSI and Neural Systems*. Only the essential results for these circuits which pertain to the wavelet transform will be presented in this paper.

8.1 Subthreshold Transistor Physics

Most of the circuits in the wavelet transform use transistors which operate in the subthreshold region (i.e., with the gate-to-source voltage below the threshold voltage of the transistor). In this region, the current-voltage characteristics of the transistor follow an exponential function, instead of the square-law function. The function which I will use for the analysis is, in its most detailed form,

$$I_{\mathrm{DS}} = \left(\frac{W}{L}\right) I_0\, e^{(V_B - V_S)(1-\kappa)/V_T}\, e^{(V_G - V_S)\kappa/V_T} \left(1 - e^{-V_{\mathrm{DS}}/V_T} + \frac{V_{\mathrm{DS}}}{V_0} \cdot \frac{L_0}{L}\right),$$

with many simplifications made for the purposes of analysis. This is known as the Vittoz-Enz transistor model [7]. Terms and constants in the above equation (and throughout the paper) are defined as follows:

I_{DS}	Current through the transistor (drain-to-source)
$\left(\frac{W}{L}\right)$	Ratio of (drawn) width to length
I_0	A pre-exponential constant (see below)
κ	Gate efficiency constant, typically about 0.7 (see below)
V_T	Thermal voltage, $\frac{kT}{q}$, or approximately 25 mV
V_G	Transistor gate voltage
V_S	Transistor source voltage
V_D	Transistor drain voltage
V_{DS}, etc.	Drain-to-source voltage
V_B	Transistor bulk (well or substrate) voltage
V_0	Early voltage
L_0	Effective channel length

In this equation, we make no use of the usual term V_t, the threshold voltage. Measurements of transistor characteristics have shown that both κ and I_0 are closely correlated both to V_t and to each other [6, 8]. κ (and therefore I_0 and V_t) is a function of V_B, but for the purposes of analysis will be assumed to be constant. Other simplifications include ignoring the Early effect and the effect of the well (or substrate) voltage, resulting in the expression

$$I_{\mathrm{DS}} \approx \left(\frac{W}{L}\right) I_0\, e^{V_{\mathrm{GS}}\kappa/V_T} \left(1 - e^{V_{\mathrm{DS}}/V_T}\right).$$

For most of the operating range of the transistor, the term in parentheses is approximately unity, and the equation becomes

$$I_{\mathrm{DS}} \approx \left(\frac{W}{L}\right) I_0\, e^{V_{\mathrm{GS}}\kappa/V_T}.$$

The simplest small-signal model used is a transconductance current source $I_{\mathrm{ds}} = g_m V_{gs}$ in parallel with a resistor g_0. The small signal parameters are calculated from the large signal parameters by

$$g_m = I_{\mathrm{DS}} \left(\frac{\kappa}{2V_T}\right)$$

and

$$g_0 = \frac{L_0}{V_0 L}.$$

g_0 is generally on the order of $2e^{-11}$, and g_m is on the order of 100 times g_0.

8.2 The Wide-Range Amplifier

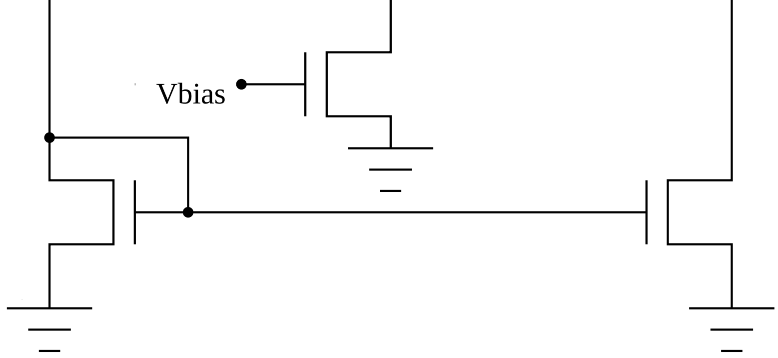

Figure 4: The wide-range differential transconductance amplifier.

The transconductance amplifier is the basic building block of almost all Analog VLSI circuits. Its schematic and symbol are shown in Figure 4. This circuit is used in two different ways: First, as a current-output device, for which the output function is

$$I_{\text{out}} = I_{\text{bias}} \tanh \frac{\kappa(V_+ - V_-)}{2}$$

and secondly as a voltage-output device, for which the (small signal) voltage gain is

$$\frac{V_{\text{out}}}{(V_+ - V_-)} \approx \frac{g_{\text{mn}}}{(g_{0\text{n}} + g_{0\text{p}})}$$

and is on the order of 200 to 300. The large-signal output voltage in this case is fixed by bias circuitry at the amplifier output. The total current I_{bias} through both sides of the differential amplifier is fixed by the bias voltage V_{bias} according to the (simplified) transistor equation $I_{\text{bias}} = \left(\frac{W}{L}\right) I_0 \, e^{V_{bias}\kappa/V_T}$; this bias is generally set to the range 0.6V to 0.8V, which keeps the transistor in the subthreshold region and restricts current through the circuit to the nanoamp range, but with the current high enough to keep the signal-to-noise ratio of the output large.

One of the major uses of the transconductance voltage amplifier is the follower, in which the negative input V_- is tied to the output V_{out}, and for which $V_{\text{out}} \approx V_+$.

8.3 The Hysteretic Inverter

This circuit, shown in Figure 5, is the low-power analog VLSI equivalent of the latch. The bias voltage V_{bias} is set to place the transistor in the subthreshold region. The limited amount of current prevents the circuit from switching very fast, so it should only be used in instances where slow switching time is acceptable. In the wavelet transform, it is used to produce the oscillatory output for the modulators, so its highest rate is on the order of 20 kHz. Where necessary, raising the bias voltage will decrease the switching time at the expense of power consumption. The switching points of the hysteretic inverter are close to power and ground,

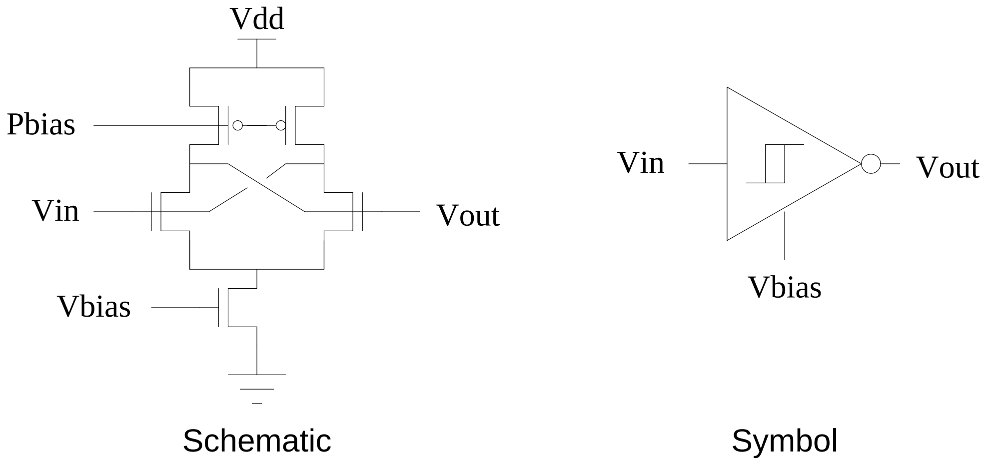

Figure 5: The hysteretic inverter/latch circuit.

and can be adjusted slightly by altering the values of P_{bias} and V_{bias}. Usual values for these parameters are $V_{\text{bias}} = 0.8$V, and $P_{\text{bias}} = 4.3$V.

8.4 Low-Gain Resistor-Amplifier

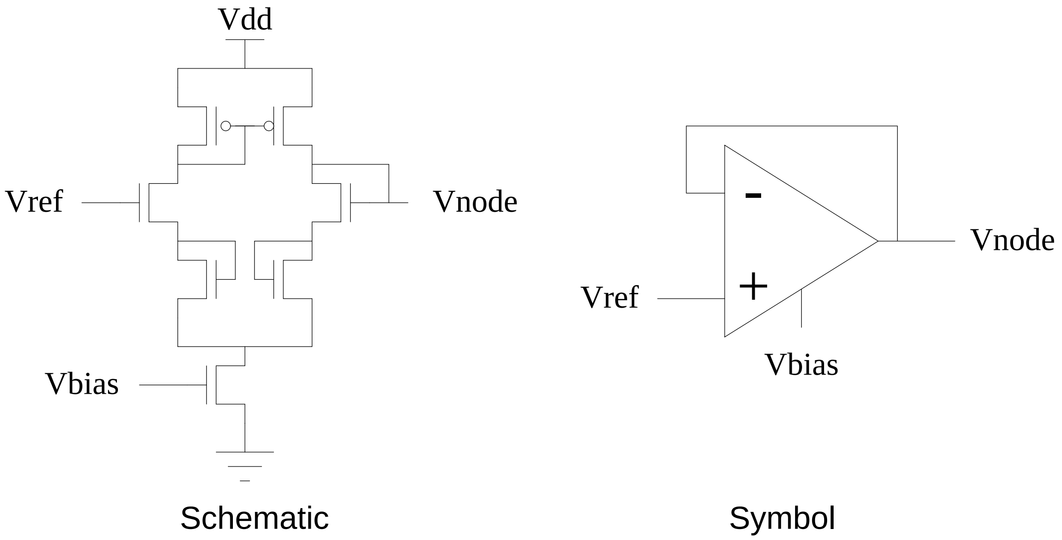

Figure 6: The resistor amplifier-follower circuit.

One of the difficulties of Analog VLSI is translating Voltages to Currents and vice versa in a linear fashion. The main problem is that the value of resistors needed is too large for a conveniently short poly line drawn on the chip, and too small for the natural resistance of a transistor fixed in subthreshold. However, in cases for which a resistance is needed from any point to a fixed reference voltage, in order to transform a current output from an amplifier or similar device into a voltage, a transconductance amplifier with fairly low gain can be acceptable. This amplifier is connected as a follower and thus acts like a follower-aggregator (Section 8.8). The purpose of forcing the amplifier to have low gain increases the region in which the effective resistance is linear. The two diode-connected transistors in the circuit add to the g_0 conductance of the input transistors which reduces the small signal voltage gain, according to the equation above.

8.5 Divide-Down Flip-Flops

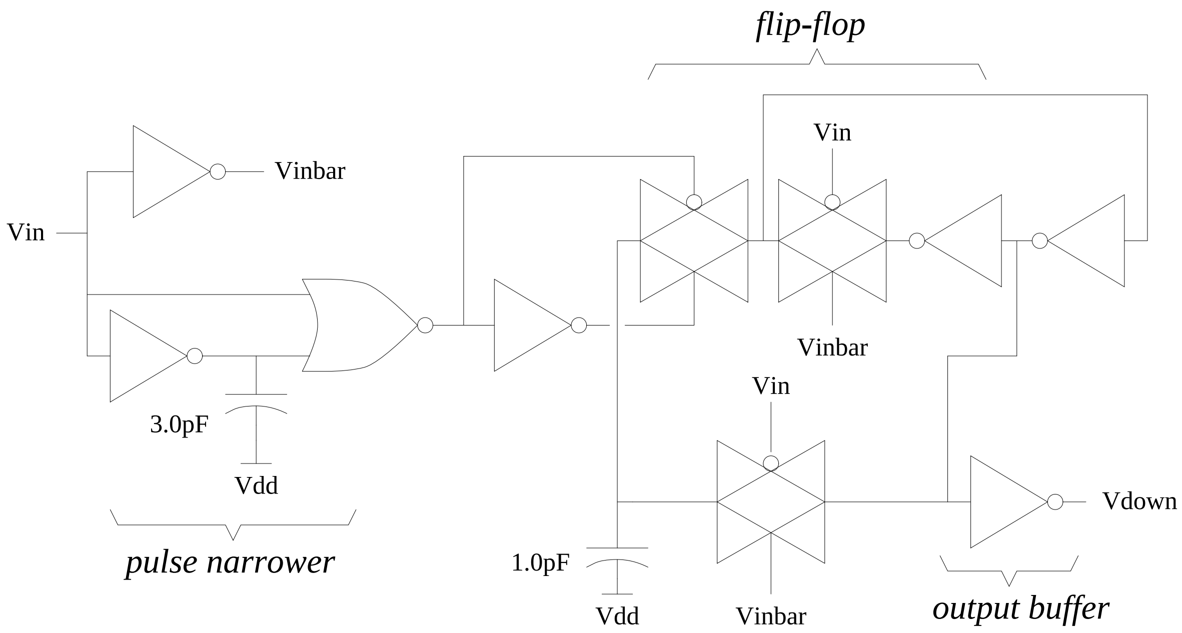

Figure 7: Divide-down flip-flop circuit.

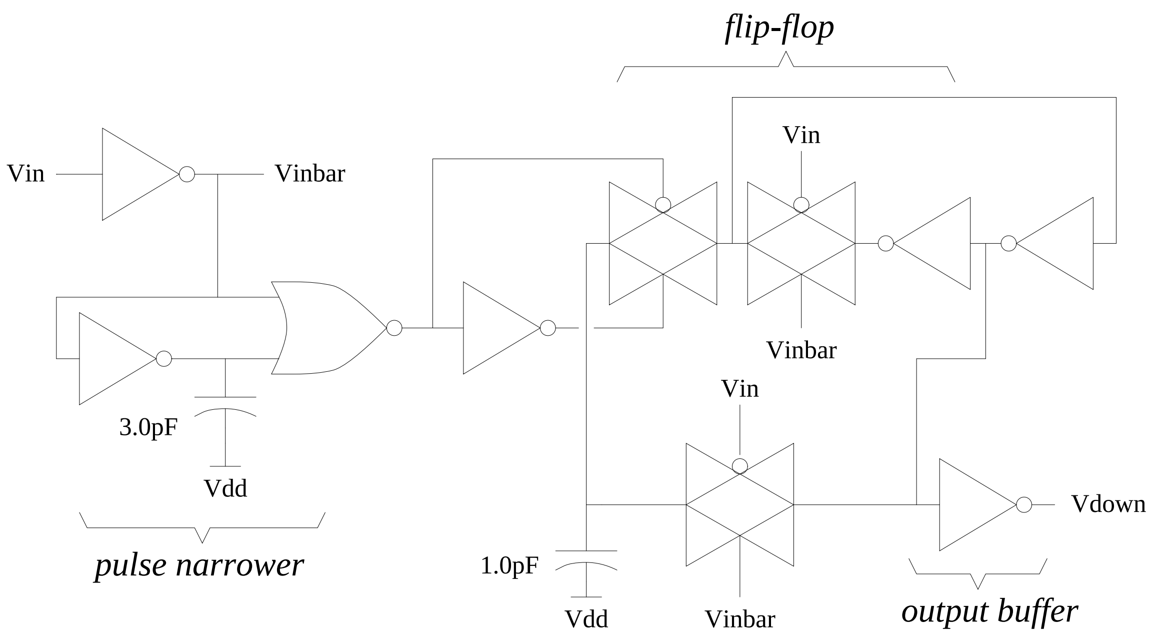

Figure 8: Divide-down phase shifted flip-flop circuit.

The function of this circuit, which is digital in nature, is easily seen from the circuit diagram. One portion of the circuit produces a short pulse whenever the input clock transitions from low to high, which creates the second part of a two-phase clock used to control the flip-flop.

Figure 8 differs from Figure 7 in that the output of one is 90° out of phase with the other, which is necessary to produce the sine and cosine signals for the demodulation process.

8.6 Wide-Range Multiplier

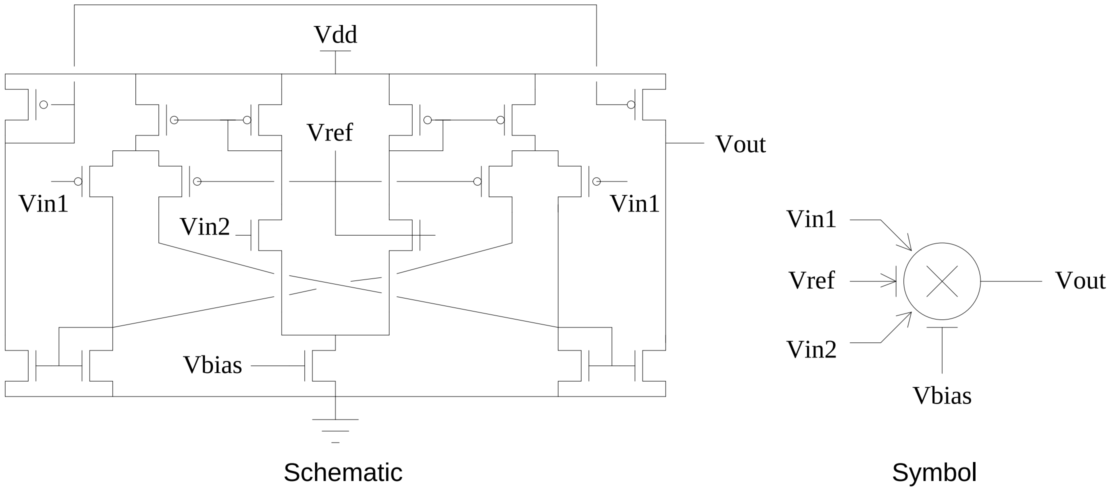

Figure 9: Wide-range four-quadrant Gilbert multiplier.

Another of the circuits analyzed in Mead's book, the output current is a multiplicative function of four differential inputs:

$$I_{\text{out}} = I_{\text{bias}} \tanh \frac{\kappa(V_{1+} - V_{1-})}{2V_T} \tanh \frac{\kappa(V_{2+} - V_{2-})}{2V_T}$$

In this case, I_b is computed from the bias voltage V_{bias} in exactly the same manner as for the transconductance amplifier. Although the output undergoes nonlinear (tanh) compression at extreme values of differential input, the tanh function is approximately linear for small values of the input.

In the wavelet transform, we wish to multiply two numbers together, both referenced to the same midrange (2.5V) value; in this case $V_{1+} = V_{2+} = V_{\text{ref}} = 2.5V$.

8.7 Second-Order Section

The purpose of the second-order section is to act as a low-pass filter with a fairly sharp cutoff frequency. The second-order section is extensively discussed in *Analog VLSI and Neural Systems*. The circuit used here contains a modification to the wiring between the three transconductance amplifiers which was invented by Neal Bhadkamkar at Stanford University [9]. The modification makes the circuit more robust but does not affect the first-order approximate function of the circuit, which has an input-to-output transfer function of

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{1}{\tau^2 s^2 + 2\tau s(1-\alpha) + 1}.$$

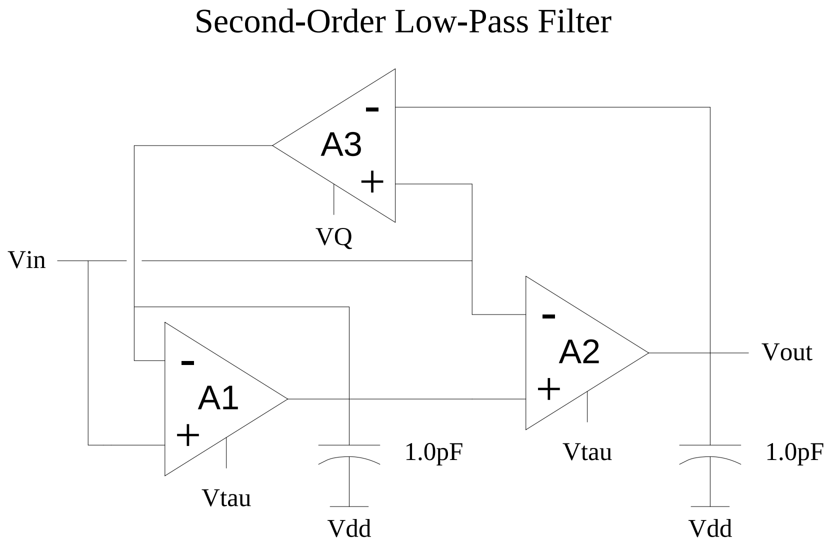

Figure 10: The second-order section low-pass filter.

The parameters are related to the input bias voltages V_τ and V_Q according to the following equations:

$$\tau = \frac{C_1}{g_{m1}} = \frac{C_2}{g_{m2}}$$

$$\alpha = \frac{g_{m3}}{g_{m1} + g_{m2}}$$

where g_{m1}, g_{m2}, and g_{m3} are the transconductances of the amplifiers labeled $A1, A2$, and $A3$ respectively. The equation relating transconductance to bias voltage is found above in Section 8.1.

8.8 Follower Aggregator

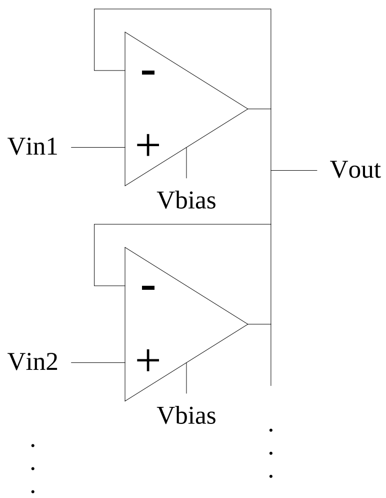

Figure 11: The follower-aggregator (input averaging) circuit.

This interesting circuit combines the definition of the amplifier as a voltage-output and a current-output device in the same circuit. While each amplifier in the aggregator attempts to follow its own input, its output is pulled to an average value of all the inputs. The outputs may be tied together because in that arrangement the current outputs from each amplifier adjust to make the total current zero according to Kirchoff's law. Each input can be weighted in relation to the others by adjusting the bias voltage on the associated amplifier. For the purposes of the wavelet chip, we always want a pure average, so the biases of all the transistors are tied together. When this is done, the equation of the output is no longer a function of the bias voltage (which should therefore be set to some reasonable value such as 0.7V to 0.8V), but is simply

$$V_{\text{out}} = \frac{1}{n}\sum_{i=1}^{n} V_{\text{in}i}$$

for n amplifiers in parallel.

8.9 Gaussian filter section

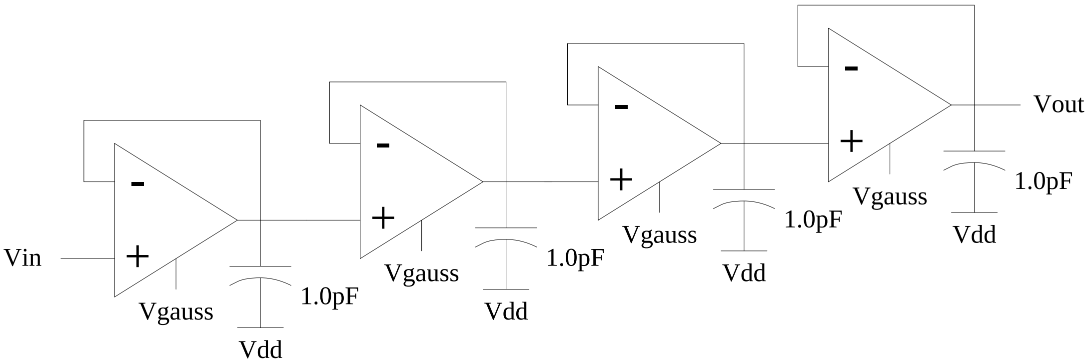

Figure 12: A four-stage filter approximating a half-gaussian function.

The equations relating to the width of the gaussian filter are discussed in Section 3. The parameter τ used in those equations is the same τ as is computed for any follower-integrator, $\tau = C/g_m$. For the five stages of this filter, we assume that the amplifiers and capacitors are matched, such that the τ for the whole filter is the same as the τ for any one amplifier. Since we want to achieve a desired bandwidth BW, and we can compute τ for any given BW, then we need to know V_{gauss}, which is easily derived from equations already presented, and is

$$V_{\text{gauss}} = \frac{V_T}{\kappa}\ln\left(\frac{2CV_T}{I_0\kappa\tau}\right).$$

8.10 Wavelet chip slice

Figure 13 shows a single "slice" of the wavelet chip. There are twelve slices in all, each containing the logic to divide down an incoming clock (oscillator) signal, low-pass filter the oscillator to produce a smooth sine (or cosine) wave, multiply this modulating signal with two different inputs (one of them for the signal decomposition part of the transform, the

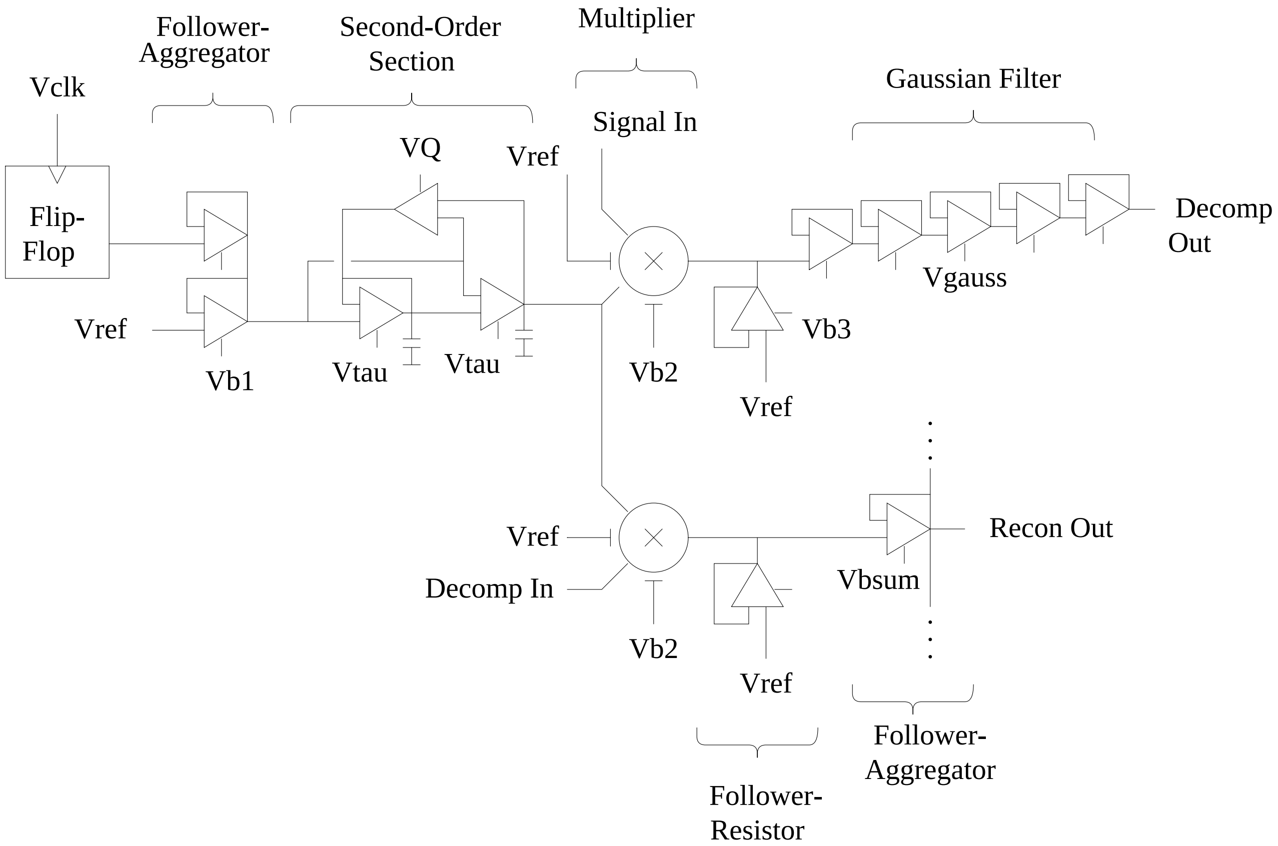

Figure 13: One of twelve slices of the wavelet transformer.

other for the reconstruction half), low-pass filter the decomposition result with a gaussian-shaped function, and aggregate (average) the reconstruction result with the result from all other slices to produce a final result. The slices alternate between those producing sine wave modulating signals and cosine wave modulating signals (only defined by their phase relation to one another). Each sine-cosine pair of slices receives the same value of V_Q and V_τ for the modulator low-pass filter, and the same value of V_{gauss} for the gaussian filter. These three values are connected along the length of the wavelet transform chip by long polysilicon resistors; when the value of V_Q, V_τ, and V_{gauss} are set properly for the first and last slices, the values for the intermediate slices are automatically linearly spaced between the endpoint values. In the chip pin description, the addition of H or L subscript on the above signal names means the high or low endpoint value (for the high-frequency modulator output or low-frequency modulator output, respectively).

8.11 Oscillator

Figure 14 shows the voltage-controlled oscillator used in this circuit. This actually consists of two oscillators; each oscillator controls the behavior of the other, so that the frequency will drift only half as much as it would for a single oscillator. The frequency f of the oscillator is proportional to the exponential bias voltage V_f. Empirical results from simulation give an equation for frequency vs. bias voltage as:

$$V_f = (.1065)\ln(f + 1).$$

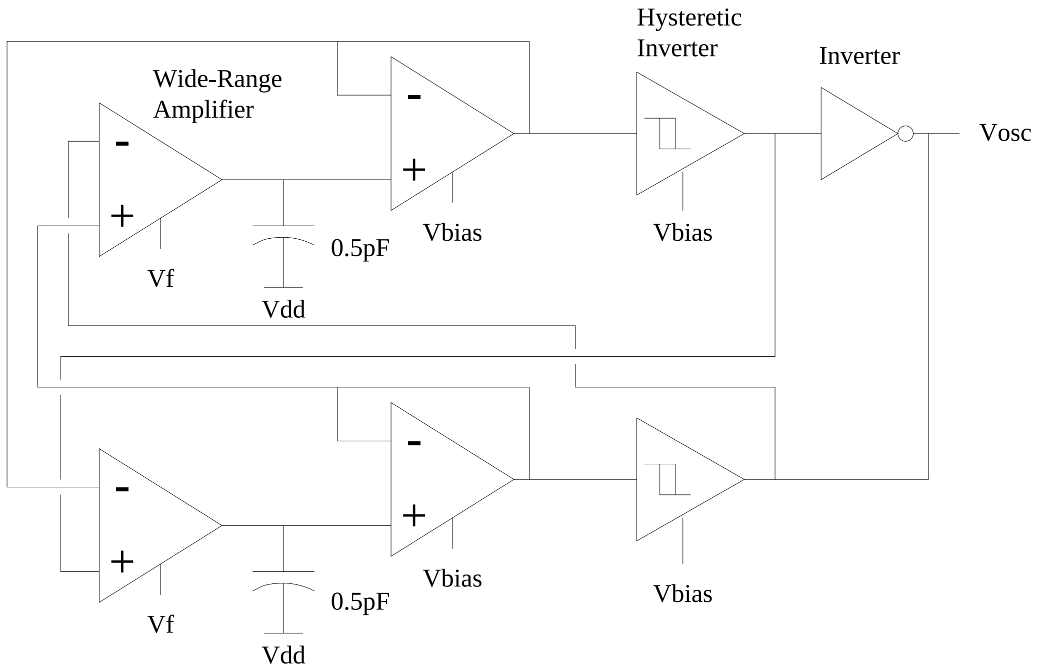

Figure 14: Low-power voltage-controlled oscillator.

The desired voltage V_f is that which produces a frequency f two times higher than the desired highest center frequency (the frequency of the first demodulating cosine/sine waves).

8.12 Miscellaneous Circuits

There are several circuits whose operation is not essential to the operation of the wavelet transform, but which provide backup services, test point observability, and increased drive capability for circuit outputs. The first of these is the external clock override. Due to the analog nature of the voltage controlled oscillator, the frequency of the oscillator output will have a slight tendency to drift due to factors such as temperature change. While a slow drift should not affect the ability of the circuit to reconstruct a signal, a stable input clock is probably desired for most applications. The signal **ExtCLK**, when high (5V), will cause the output of the oscillator to be shut off from the rest of the circuit, and the input from the signal **CLK** will drive the chain of flip-flops directly. The frequency of **CLK** should be twice that of the highest desired center frequency. The external clock is also necessary in case an unusually high center frequency is desired, because the switching speed of the hysteretic inverter limits the maximum frequency which the oscillator can produce.

The signal $\overline{\textbf{TEST}}$, when set low (0V), causes each of the twelve decomposition outputs to be directly connected back to the reconstruction inputs, creating a direct loopback which ideally should produce a perfect reconstruction of the input. While $\overline{\textbf{TEST}}$ is low, the reconstruction input pins and decomposition output pins are isolated from (unavailable to) the system. This circuit is shown in Figure 16.

All test points, decomposition output signals, and the final reconstructed signal are

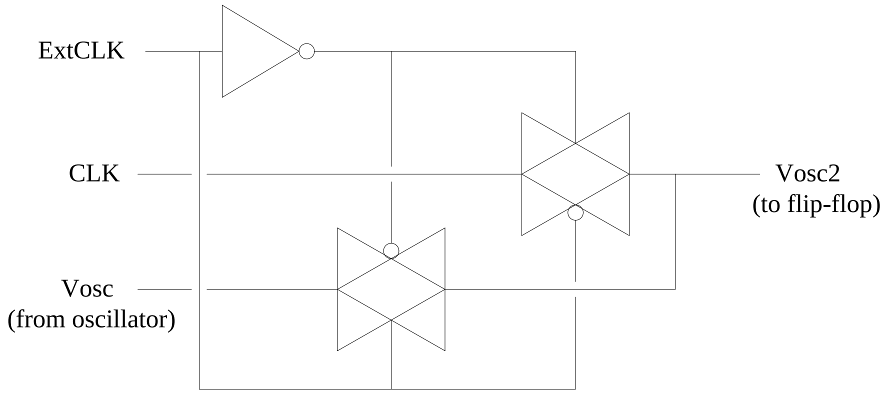

Figure 15: External Clock override logic.

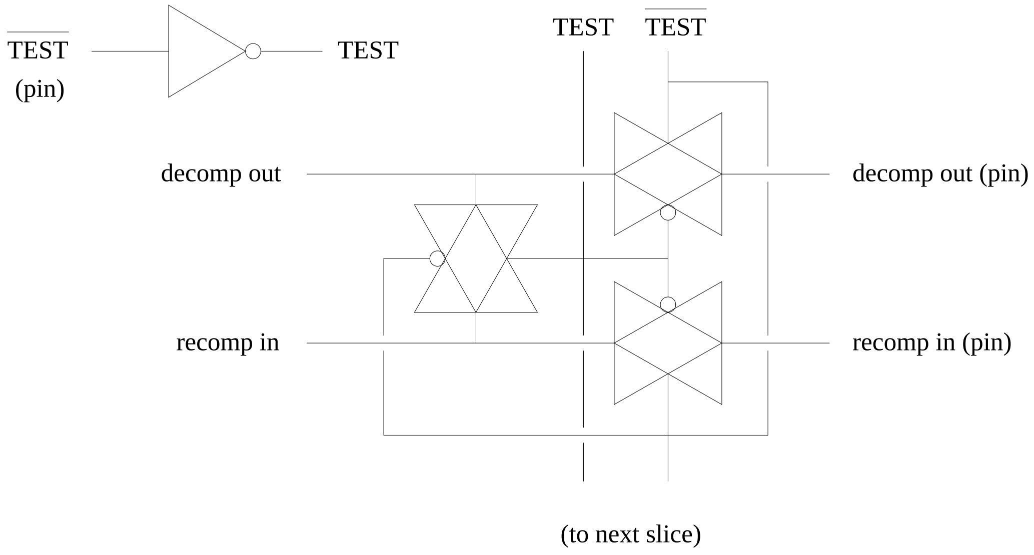

Figure 16: Test Mode logic.

buffered with a single wide-range amplifier in order to better drive the pad capacitance. Each of these amplifiers is biased with the signal **Vdrive**, set at rougly 2.6V in order to provide a fairly large current output from the transconductance amplifier.

9 Using the Wavelet Chip

Since the theoretical results are only approximations, we expect to set the operating voltages on the chip piece by piece, according to given test procedures.

1. **Setup procedure:** Until otherwise notified, $\overline{\textbf{TEST}}$ should be set high (5.0V). This signal works as described above. The other lines which must be set before beginning the test procedures are **Vdd** (5.0V), **GND** (0.0V), and **Vdrive** (2.6V).

2. **Testing the Flipflops:** This test will confirm the clock range over which the flipflops operate correctly. Set **ExtCLK** high, and attach input **CLK** to a function generator generating a variable-frequency square wave between 0 and 5 volts. Display the signals **CosOscTest**, **SineOscTest**, and **CLKout** on and oscilloscope in addition to the input function generator signal. **CosOscTest** should be at half the frequency of the input, **SineOscTest** should be at the same frequency but leading **CosOscTest** by one-quarter of a period, and **CLKout** should be oscillating at 1/64 the rate of the input. Determine the frequency range of correct operation.

3. **Testing the Oscillator:** Set **OscPbias** to 4.3V, **OscVbias** to 0.8V, and **Vf** to a voltage generator. Attach **DblOscTest** to an oscilloscope. Set **ExtCLK** low to disable the external clock. Set **Vf** to a value of 0.7V. This should produce a square wave on the oscilloscope. Vary **Vf** and measure frequency at a few different points. Find the maximum and minimum frequencies at which the circuit will behave properly. Make sure that **CLKout** is still producing a square wave at 1/64 the rate of **DblOscTest**.

4. **Testing the Modulator LPF:** Continue to generate a square wave input to the circuit using a signal on the external clock as outlined in test number 2 above. Set **VrefD** to 2.5V. Set **Vb1** to 0.8V. Set the external clock rate to the rate at which the wavelet chip will be expected to operate. Set **VtauH** to about 0.61V and **VQH** to about 0.60V. Leave **VtauL** and **VQL** disconnected. Attach the signal **CosWaveTest** to an oscilloscope. Adjust the values of **VtauH** and **VQH** until the output best matches a sinusoid. Generally, **VtauH** should remain about 0.01V higher than **VQH**. Modify the gain using **Vb1** (and also **VQH** and **VtauH** if necessary) to set the peak-to-peak amplitude of **CosWaveTest** to about 0.4V. Repeat the test for an external clock rate of 1/32 of the first test. When done, set **VtauH** and **VQH** to the values determined from the first test, and **VtauL** and **VQL** to the values determined from the second test.

5. **Testing the Modulator Multiplier:** Initially set pins **Vb2** and **Vb3D** to 0.8V each. All other pins should remain as they have been set from the previous tests. This test is important to keep the output of the multiplier from overflowing. Attach pin **Vin** to **VrefD**, and the pin **MultTest** to an oscilloscope. The output **MultTest** should be nearly constant and equal to 2.5V. If there is a significant signal through the multiplier due to mismatched transistors in the current mirrors, adjust **VrefD** until

it disappears. Record the new **VrefD** value. Now, generate a sine wave centered at 2.5V (**Vref**), having a peak-to-peak amplitude of 0.4V. The output **MultTest** should be a signal containing the sum and difference of the function generator sinusoid and the **CLK** input (or the output from the voltage-controlled oscillator, if that is being used instead). Adjust **Vb3D** until the multiplier output is well-behaved, and if the output is greater than 0.4V peak-to-peak, adjust **Vb3D** until it is limited to that amount.

6. **Testing the Gaussian Filter:** In order to set the proper width for each gaussian filter section, set **Vin** to a constant of about 0.2V. Attach the external clock pin **CLK** to a function generator. For several values of **VgaussH** in the range of about 0.4 to 0.7, measure the amplitude of the output (**DecompR1** or **DecompI1**) over a range of input frequencies starting from about 50Hz. Record the -3dB cutoff point for each value of **VgaussH** to get an accurate measure of width (or rather half-width) vs. bias voltage. When finished, return the signal **CLK** to its normal operating frequency, and set pins **VgaussH** and **VgaussL** to the proper values (namely, half-width = $3/4 \times$ the center frequency). Relate the experimental result to the theoretical result given above. With the settings above, confirm that the modulation signal is seen at each of the twelve outputs, and that the amplitude is rougly equal for all channels.

7. **Testing the Recomposition Output:** Set the $\overline{\textbf{TEST}}$ line low (0.0V) in order to attach the decomposition outputs directly to the reconstruction inputs. Connect **Vb3R** to **Vb3D**, and **VrefR** to **VrefD**. Set **Vbsum** to about 0.8V. Attach **Vin** to a function generator and **Vout** to an oscilloscope. Generate a sine wave of 0.4V p-p amplitude at the input, centered around **VrefD**. Confirm that for all inputs in the range of the transform bandwidth, the reconstructed output is approximately equal to the input. If there is some oscillating signal at the output when **Vin** is at a DC (constant) value, then separate **VrefR** from **VrefD** and adjust its value until the spurious oscillations quit. If the output is highly nonlinear, separate **Vb3R** from **Vb3D** and decrease its value until the output becomes linear. Note that there may be a constant gain difference between the original and reconstructed signals.

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